

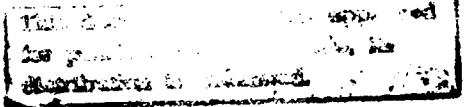
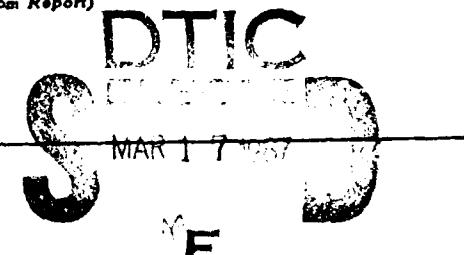
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charged-device modeling. As such, contrary to the popular notion that rugged bipolar devices are not excessively prone to ESD-based detrimental effects, SOE transistors, on the other hand, are severely vulnerable to EOS threats. It is not just the Wunsch-Bell limit of catastrophe due to PN junction burnout (under high-level zaps) that dictates the damages in the devices like SOE transistors. The entire device configuration, namely, active junction, metallization, bonding, etc., as well as the external packaging, decide the device lethality. This is demonstrated by experimental studies on a family of SOE devices by subjecting them to ESD zaps using a Human Body Simulator. The results positively indicate that their vulnerability is in excess of Class II limit specified by DOD-HDBK-263 and require specific handling precautions, lest they would pose quality control and/or field failure problems. Especially, considering these devices being extremely costly, specific ESD control efforts are rather imminent.

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**ESD/EOS SUSCEPTIBILITY OF A CLASS OF BIPOLEAR RF POWER TRANSISTORS:
EXPERIMENTAL STUDIES ON STRIPLINE-OPPOSED EMITTER TRANSISTORS**

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ABSTRACT

Susceptibility of a class of bipolar RF power transistors (known as stripline-opposed emitter (SOE) devices) to electrical overstressing (EOS) is studied. By virtue of having unique packaging compatible for RF/stripline applications, SOE devices pose prominent/extended exteriors for static propensity and hence are critically vulnerable to damages/degradation as predictable by the charged-device modeling. As such, contrary to the popular notion that rugged bipolar devices are not excessively prone to ESD-based detrimental effects, SOE transistors, on the other hand, are severely vulnerable to EOS threats. It is not just the Wunsch-Bell limit of

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INTRODUCTION

This work addresses the proneness to ESD/EOS of certain bipolar devices used in RF power amplification, commonly known as stripline-opposed emitter (SOE) transistors. These devices have characteristic packagings as depicted in Fig. 1. They are silicon transistors designed for high efficiency, high linearity Class A-power amplification at UHF bands [1].

The primary electrical advantage of the SOE packages are the low inductance stripline leads which interface very well with the microstriplines often used in UHF/VHF equipment and the good collector to base isolation provided by the two emitter leads. The two-emitter concept promotes symmetry in board layout when combining devices to obtain higher

power output. Further, stud and/or flange-mounting feasibility of SOE devices permit excellent heat-sinking and hence high thermal performance.

While the aforesaid characteristics allow popular use of the SOE devices for the purpose of RF power amplification, there is no available data regarding their performance under electrostatic discharge (ESD)/electrical overstressing (EOS) environment. Like any bipolar device, per DOD-HDBK-263, these devices may, in general, fall under Class II category [2] of components in respect of their ESD/EOS proneness. However, this generalization needs to be verified because the peculiar package-geometry pose a prominent/extended cross-section of exposure to the static environment. As such, the severity of ESD damage in such bipolar devices would be reduced not only by the Wunsch-Bell limits of catastrophe [3] at the PN junction [4], but also by the static propensity and parasitic (shunt) paths of static-discharge associated with the device package. Further, the inherent capacitive and/or inductive reactance of the device-exterior will profusely influence the static discharge characteristics and hence the relevant ESD-based stressings on the device.

Thus the present work will decide whether SOE packaged bipolar devices be classified under general Class II type of ESD-prone components as listed in the DOD-HDBK-263. Relevant effort will also explicitly determine the effect of performance-based packaging on the device vulnerability to ESD/EOS.

In SOE devices, the junctions are designed enough to carry a sustained current flow of about 1 ampere, compatible for high power applications. Therefore, the possibility of total junction burnout (Wunsch-Bell limit) by ESD zaps may not be anticipated. However, considering the total device geometry (with its constricted regions, bond/metallization regions, etc.), vulnerability of the device to ESD-based damages cannot be ruled out, especially due to the presence of high static propulsive exterior (packaging). Hence, the present investigations are done on the devices subjecting them to simulated ESD zaps to evaluate their proneness to EOS damages.

EXPERIMENTAL STUDIES

The test transistors considered are: ENI 10A, ENI 14B and ENI 2240. These devices form a class of bipolar active elements intended for applications with high performance thermal and high frequency characteristics. They have typical stripline opposed emitter (SOE) packaging designed for interfacing with microstriplines and for good thermal dissipative capabilities.

Prezap Tests:

The static characteristics, as well as the transistor gain h_{FE} , were measured prior to the application of zaps. The unstressed device

characteristics indicate that for a given type of transistor, the reverse-bias leakage current varies widely from piece-to-piece at ambient conditions. The reverse breakdown also ranged from abrupt to smooth artifacts. In some cases, ohmic short across base-emitter (B-E) junctions were observed.

The prezap test results are presented in Tables 1 to 3 and the prezap test is labelled as 'a' in the test sequence.

Zap Tests:

The zap tests were performed on the devices using an ESD human-body simulator (Model: IMCS2400). This equipment simulates the transient discharge characteristics which is a close representation of the ESD event pertaining to the static discharge from a human body. The simulator circuit (per MIL-M-38150) [2] is depicted in Fig. 2.

Testing methods are documented [2] in DOD-HDBK-263, Art. 6.2. Normally ESD-based part failure is defined as the inability of a part to meet the electrical parameter limits of the part specifications. Any measurable change in a part electrical parameter due to an ESD could like an indication of part damage and susceptibility to further degradation and subsequent failure with successive ESD.

Hence using the standard ESD Simulator (Model: IMCS2400), the test devices were subjected to various combinations (in terms of polarity, amplitude, multiplicity, etc.) of ESD zaps. (Prior to overstressing, the devices were assessed for their characteristics, as mentioned earlier under 'Prezap Tests').

The characteristics of the devices after each mode of test were measured using the Semiconductor Parameter Analyzer Model: HP4145. These results are presented in Tables 1-3. The sequence of tests conducted after overstressing are referred to as b, c, d, e, f, and g.

Tables 1-3 provide the complete compilation of test data and summarize the results. The recorded characteristics are depicted in a few sets of figures appended. Each set of figures is identified by the device type/number, the sample number, and the test sequence. For example, Fig. A 1.b denotes the characteristics of the transistor A (ENI 10A), sample number 1, after the overstressing sequence of 'b,' as described in Table 1. Likewise, B refers to transistor ENI 14B, and C denotes ENI 2240.

OBSERVATIONS

- a. The tested devices are prone to ESD-based failures and/or degradations.

- b. Low level zaps cause no catastrophic damages. However, the devices are susceptible for catastrophic failures at high zap levels which can be anticipated at low humidity situations.
- c. The degradation is cumulative but stabilizes after a few multiple zaps. Up to 20% change in h_{FE} and a more serious variation of I_{EBO} (leakage current) changing in excess of 100% were observed.
- d. Polarity Dependence: Zaps of alternating polarities appear to influence the degradation to a larger extent. (The probabilities of occurrence of positive and negative zaps can be anticipated to be the same in practice.)
- e. Multiple single polarity zaps of larger magnitude do not cause more harm than low intensity, multiple zaps of bidirectional polarity.
- f. Isolated single zaps appear to cause no damage (even on already wounded devices).
- g. Frequent manual handling of the devices with the possibilities of applying zaps of bidirectional polarities in a sequence, would damage them to a maximum extent.

- h. The devices are more prone to damages while receiving a set of initial zaps. Subsequent zaps may not influence any further degradation. However, the devices pose high probabilities of receiving initial zaps anywhere in the production/manufacturing, shipping or assembly lines.
 - i. The devices can be subjected to harmful zaps at subassembly/PCB levels. However, their chances of getting degraded by single or multiple zaps at equipment level are rather remote.
 - j. Devices which exhibit base-emitter ohmic leakage during prezap screen, have been observed to suffer higher damages, even at low or subcatastrophic ESD levels.
- k. Description of observed damages in these test devices:

Noncatastrophic ESD-Human Body model zaps applied between the base and the emitter of the transistors with serial numbers ENI 10A and ENI 14B caused these devices to exhibit lower h_{FE} and/or larger base-emitter junction leakage current. ESD pulses that forward biased the B-E junction, lowered the h_{FE} without significantly increasing the leakage current while pulses of reverse biasing polarity degraded the B-E junction's characteristics invariably without affecting the transistor gain at nominal current levels.

ESD pulses of reverse polarity did also affect the low current level transistor gain. The observation can be explained as follows:

1. When a reverse biasing ESD pulse is applied to the junction, most of the power dissipation occurs within the depletion layer where the electric field intensity is maximum. The temperature rise and the subsequent crystal damage in the form of increased recombination/generation centers can be anticipated to be very high in the vicinity of the junction. Therefore, junction leakage current which is predominately controlled by carriers that are generated within the depletion region increases.
2. The transistor gain at nominal current levels does not depend on depletion layer parameters and therefore, it is not sensitive to reverse biasing ESD pulses.
3. The reason for transistor gain being lower at low current densities is the significant loss of injected carriers by recombination across the B-E junction's depletion layer; this parameter drops when reverse biasing ESD pulses are applied to the junction.

4. The test transistors are made by planar technology. The curved edges of the junctions are the most vulnerable regions in reverse bias; the reverse breakdown occurs first at these edges and most of the ESD transient current flows through edge regions.

The rest of the junction, as well as the bulk of the emitter and the base, are however, much less affected. As the transistor gain at nominal current depends mainly on what occurs in these regions, this parameter is not very sensitive to ESD pulses of reverse polarity.

5. The transient current during forward biasing due to ESD zaps flows through the entire junction area and degrades the bulk of the emitter and the base, thus affecting h_{FE} at all current levels.

The catastrophic failures observed with the transistors ENI 10A and ENI 14B are due to the (emitter) contact metallization penetrating into silicon and introducing an ohmic low resistance path across the B-E junction. This metal-silicon alloy spike(s) penetrate deep into the base, even reaching the base-collector junction depletion layer, thus, severly affecting current-voltage characteristics at this junction.

Regarding the transistor ENI 2240, the observed latent failures were due to an increased wire/thin film and/or thin film metallization/silicon contact resistance. Both the emitter and the base contacts displayed this sort of vulnerability to ESD zaps. The contact fatigue increased gradually with repetitive ESD zaps, resulting in an undue increase in contact resistance values. As a result, larger V_{CE} values were needed to pull the transistor out of saturation (an increasingly larger portion of the applied V_{CE} dropped at the contacts, rather than appearing across the internal PN junctions). The excessive Joule heating at the contacts resulted in the penetration of the thin film metallization into the silicon. Low resistance paths were found across the B-E and/or B-C junction of the devices that suffered catastrophic failures.

DEVICE HANDLING: SUGGESTIONS

1. Inasmuch as the test devices indicated proneness to wounding and/or catastrophic failures under ESD zaps, proper handling procedure is suggested.
2. Though classified as Class II, the test devices being costly semiconductors be packaged, transported and handled with necessary care as specified in DOD-HDBK-263.

3. Part Screening: Some of the devices tested exhibit bypass leakage characteristics across B-E junction (e.g. ENI 10A) prior to zapping. This could have resulted from improper handling (?). Another test piece having normal prep zap characteristics was zapped (ESD-HBM Test Voltage 16KV peak, multiple) and showed similar wounded ohmic characteristics. Therefore, it is suggested that for reliable circuit operation, devices which could have been damaged earlier either due to ESD or otherwise may be screened out via simple base-emitter I-V characteristic tests enabling the rejections of damaged pieces.
4. ENI 2240 shows contact and/or metallization based vulnerability to damages under EOS. Test results indicate contact and/or metallization resistance increasing cumulatively with number of zaps. Hence, it limits the I_c max capability of the device to a significant extent and makes it unsuitable for large-signal applications. Both emitter and collector pose the above enhanced contact/metallization resistance problem. In this point of view, use of ENI 2240 may be carefully reviewed.

REFERENCES

- [1] Motorola Semiconductors: Product Review on MRF Series

- [2] DOD-HDBK-263: Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment.
- [3] D.C. Wunsch and R.R. Bell: Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors due to Pulse Power Voltages, IEEE Trans. Nucl. Sci., NS-15(6), pp 244-259 (1968).
- [4] W.J. Orvis, et al: A Review of the Physics and Response Models for Burnout of Semiconductor Devices, Final Report: UCRL-53573, Lawrence Livermore National Laboratory, UCLA, CA 94880, (December 1984).

Sample No.	Measured Pre zap Data	ESD - Human Body Model Zap Tests & Results						Comments	Remarks
		Test Sequences							
Type	I _{EBO}	80 mA	b	c	d	e	f	g	
1 45	I _{HFE}	1μA	Parameters Tests 5 zaps @ +50V to +16KV 16KV Assorted	25 zaps @ +16KV	5 zaps @ -16KV	15 zaps @ 16KV	-	-	1 For all the devices zaps are applied
-5.6V			No Change	40	36	Catastro- -phic	-	-	Base-Emitter Short
2.3μA	I _{EBO}		No Change	No Change	2.7μA	Damage	-	-	
2 47	I _{HFE}	5 zaps @ 50V to +16KV + Assorted	5 zaps @ 20 zaps @ +10KV +16KV	15 zaps @ +16KV	15 zaps @ -16KV	5 zaps @ +10KV -16KV	-	-	2 between Base & Emitter unless otherwise specified
-5.6V	I _{EBO}		No Change	No Change	No Change	No Change	23 SONA	Damage	
100μA			No Change	6.5μA	7.5μA	No Change	125μA	-	
3 44	I _{HFE}	Parameters Tests 5 zaps @ 10KV & -10KV + Assorted	30 zaps @ +10KV	5 zaps @ -16KV	-	-	-	-	a) PreZP test indicates Relevant to ohmic B-E leakage (23K JL)
-2.5V	I _{EBO}		No Change	No Change	Catastrophic Damage	-	-	-	b) the measured graphical
1.2 A			450 μA	No Change	-	-	-	-	Base-Emitter Short (80 Ohms)
4 44	I _{HFE}	Parameters Tests 5 zaps @ +7KV	10 zaps @ +7 KV	70 zaps @ +7 KV	-	-	-	-	data are depicted in Figs. A.1.a to Figs. A.1.e
-2.5V	I _{EBO}		No Change	40	No Change	-	-	-	to A.5.d
8μA			No Change	No Change	No Change	-	-	-	
5 43	I _{HFE}	Parameters Tests 50 zaps @ +7 KV	10 zaps @ +7 KV	70 zaps @ +7 KV	-	-	-	-	
-2.5V	I _{EBO}		No Change	40	No Change	-	-	-	

DEVICE UNDER TEST, EN114B RF POWER TRANSISTOR #8

TABLE 2

DEVICE UNDER TEST: ENI 143 RF POWER TRANSISTOR IB

TABLE 2

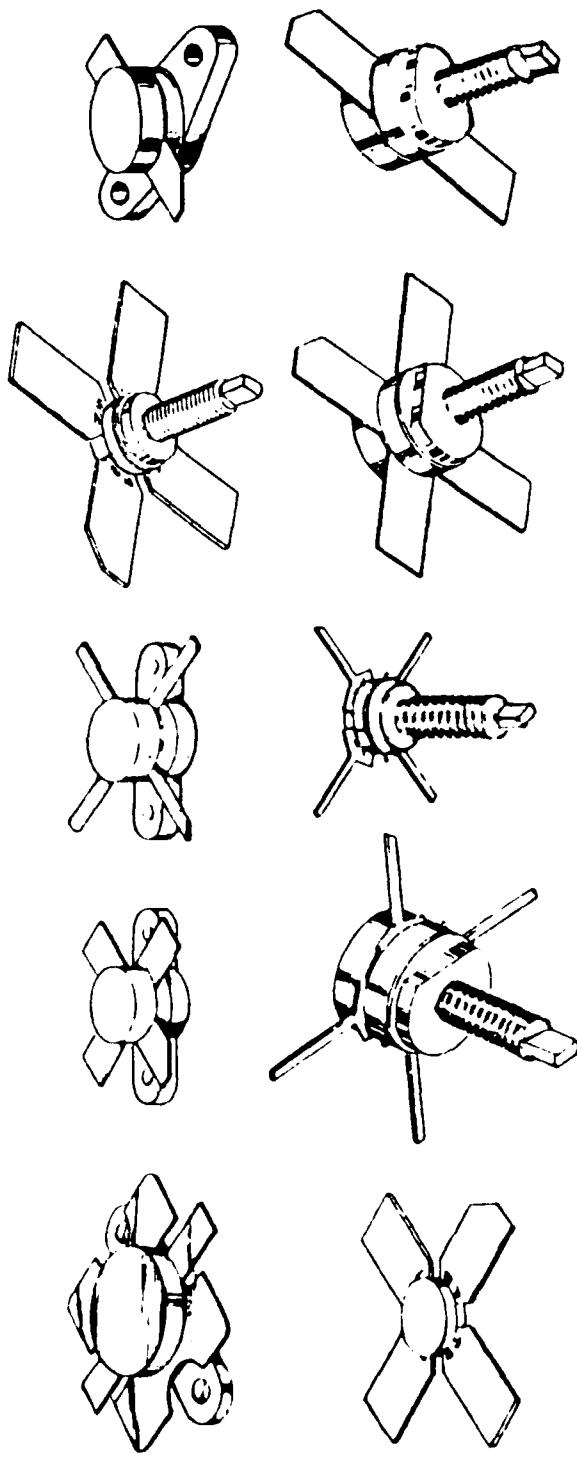
Sample No.	Measured Result Data &	ESD - Human Body Model Zap Tests & Results										Remarks
		Test Sequences					Comments					
	h_{FE} @ 80 MA	I_{EBO}	b	c	d	e	f	g				
1	44	2.1A -2V	Parameters Tests	5 zaps @ -50V to -5 -16KV (Analogous)	25 zaps @ -16KV	70 zaps @ -16KV	20 zaps @ +16KV	40 zaps @ +16KV	1.	For all the devices zap sequences applied between Base and Emitter unless otherwise specified.		
2	56	1.30A -2V	h_{FE}	No change	No change	No change	34	No change	-	-	-	
3	55	1.81A -3V	I_{EBO}	No change	5.2mA	7.5mA	6mA	No change	No change	-	-	
4	S1	1.24A -3V	Parameters Tests	5 zaps @ -50V to -16KV (Analogous)	10 zaps @ -16KV	30 zaps @ +16KV	10 zaps @ -16KV	-	2.	Relevant to the test sequences indicated the measured graphical data are presented in figs. B.1-a to B.4-e		
			h_{FE}	54.5	53	53	No change	No change	-	-	-	
			I_{EBO}	170mA	200mA	250mA	No change	No change	-	-	-	
			Parameters Tests	5 zaps @ -50V to -16KV (Analogous)	35 zaps @ -16KV	15 zaps @ +16KV	-	-	-	-	-	
			h_{FE}	No change	No change	No change	-	-	-	-	-	
			I_{EBO}	No change	No change	No change	-	-	-	-	-	
			Parameters Tests	5V CE zaps @ +500V to +16KV	10V CE zaps @ +16KV	5V CE zaps @ -16KV	20V CE zaps @ +16KV	-	-	-	-	
			h_{FE}	No change	No change	No change	No change	No change	-	-	-	
			I_{EBO}	No change	No change	No change	No change	No change	-	-	-	

TABLE 3

ESD - Human Body Model Zap Tests & Results

Sample No.	Measured Pre zap Data				Test Sequences					Comments	Remarks
	h_{FE}	I_{EBO}	$V_{CE\ sat}$	$R + R_B$	b	c	d	e	f		
1 49.4	6 μA 0.7V -2.5V 80 MA	0.7V 80 MA 0.5V 20 MA	$V_{CE\ sat}$ (Mar-ginal)	$R + R_B$ Contact Resis-tance	Parameter Tests 90 zaps @ 7KV No change	65 zaps @ 16KV 48.6	15 zaps @ 16KV $I_{Cmax} = 65\text{ mA}$	7 zaps @ 16KV $I_{Cmax} = 25\text{ mA}$	2 zaps @ 16KV ?	-	1 All zaps are applied between Base and Emitter unless otherwise specified.
2 48.6	6.8 μA 0.7V -2.5V 80 MA	0.5V 20 MA	$V_{CE\ sat}$ (Mar-ginal)	I_{EBO} No change	No change	1.1V @ 80 MA 0.5V @ 20MA	5.6 μA 0.9 @ 20 MA	5.3 μA 1.4V @ 20 MA	1 μA ?	-	2 Relevant to the test sequenced indicated measures graphical data are shown in Figs. C.1.e to C.3.c.
3 15	15 μA 70 MA	0.8V -2.5V 70 MA	$V_{CE\ sat}$ (Mar-ginal)	$(R + R_B)$ Not measured	Not measured	20 ohms	45 ohms	700 ohms	-	-	-
				Parameter Tests 5 zaps @ -50V to -16KV Assorted	25 zaps @ -16KV No change	30 zaps @ -16KV No change	-	-	-	-	-
				h_{FF}	No change	No change	Catastrophic Damage	-	-	-	-
				I_{EBO}	No change	No change	-do-	-	-	-	-
				$V_{CE\ sat}$	No change	0.9V @ 80MA 0.5V @ 20MA	-do-	-	-	-	-
				$(R + R_B)$	Not measured	Not measured	-do-	-	-	-	-
				Parameter Tests 40 V CE zaps 50 V CE zaps @ +7KV	40 V CE zaps 50 V CE zaps @ +16 KV	-	-	-	-	-	-
				h_{FE}	No change	?	-	-	-	-	-
				I_{EBO}	-do-	No change	-	-	-	-	-
				$V_{CE\ sat}$	-do-	?	-	-	-	-	-
				$(R + R_B)$	-do-	Stayed marginal	-	-	-	-	-

FIGURE 1 - SOE Packages



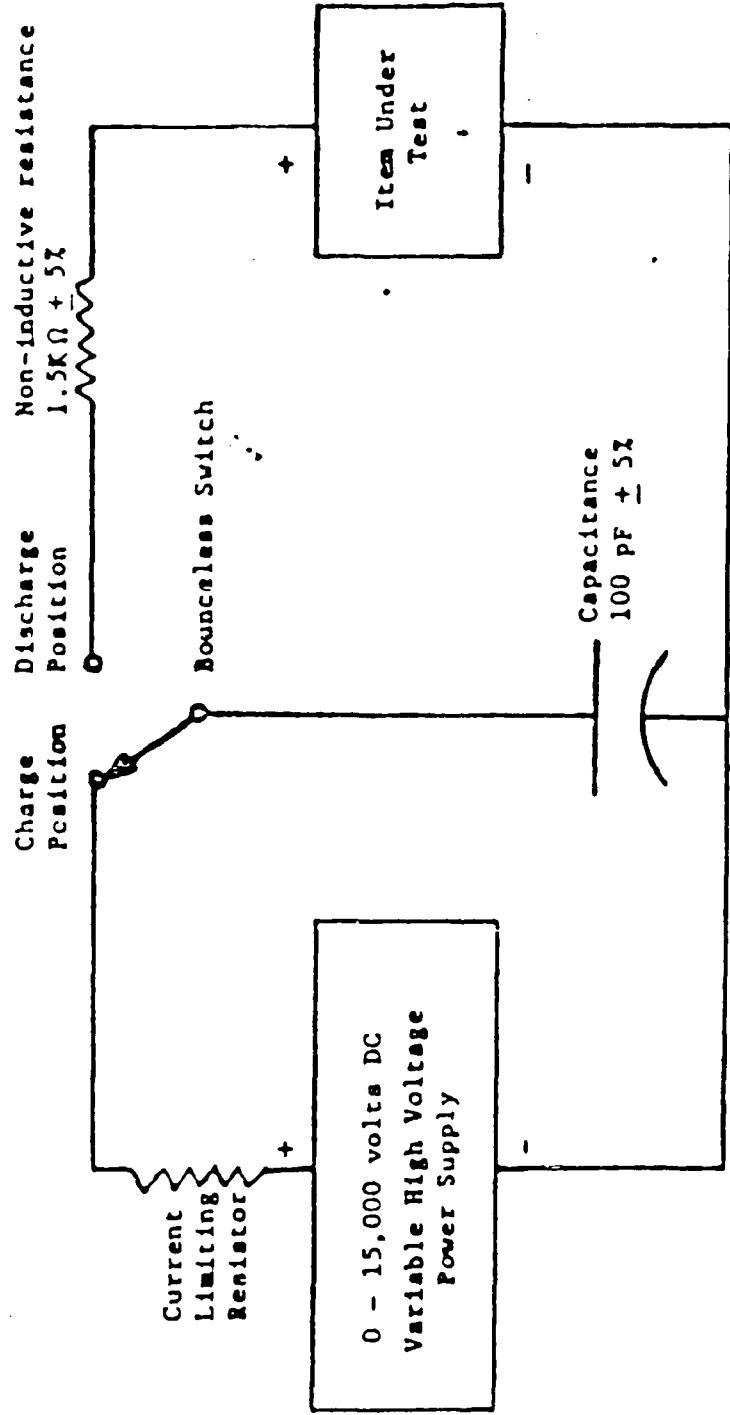
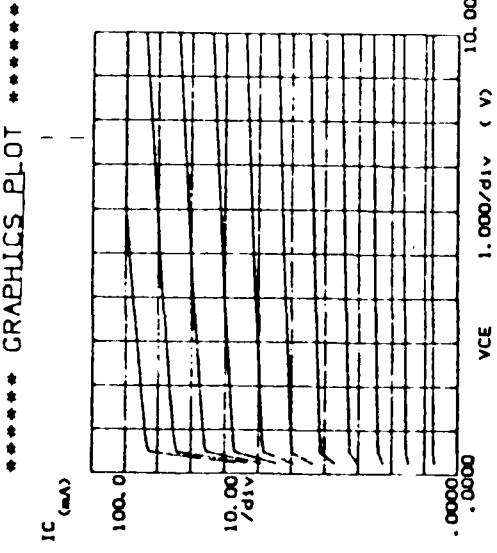
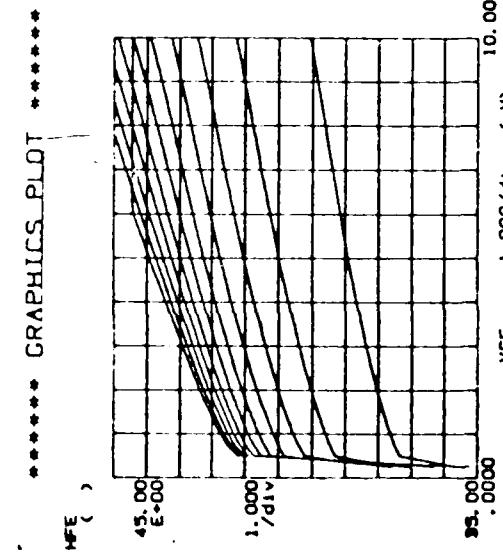


FIGURE 2. ESD test circuit

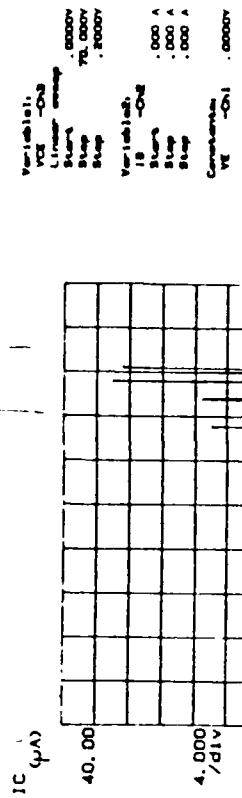
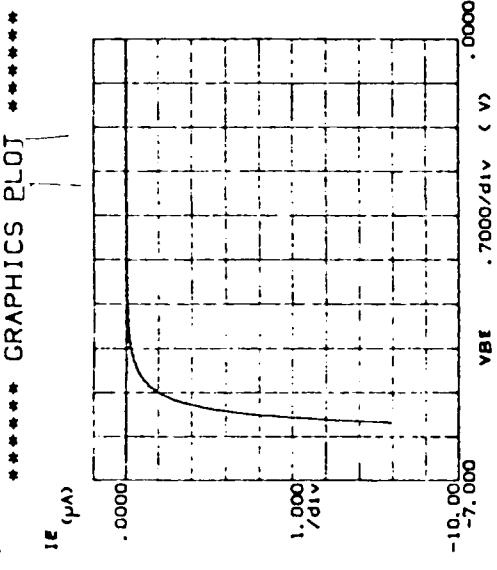
NOTE: Test voltages are measured across the capacitance. The capacitor shall be discharged through the series resistor into the item under test by maintaining the bounceless switch to the discharge position for a time no shorter than required to decay the capacitor voltage to less than 1 percent of the test voltage or 5 seconds, whichever is less. Power supply voltage shall be within a tolerance of \pm 5 percent of test voltage.

Figs. A.1.a





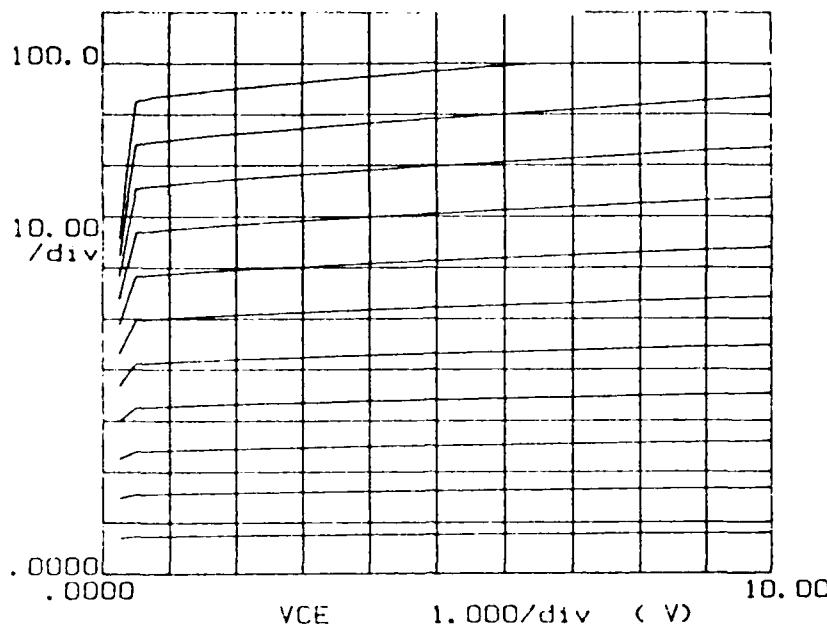
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Figs. A.1.b

***** GRAPHICS PLOT *****

IC
(mA)



Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

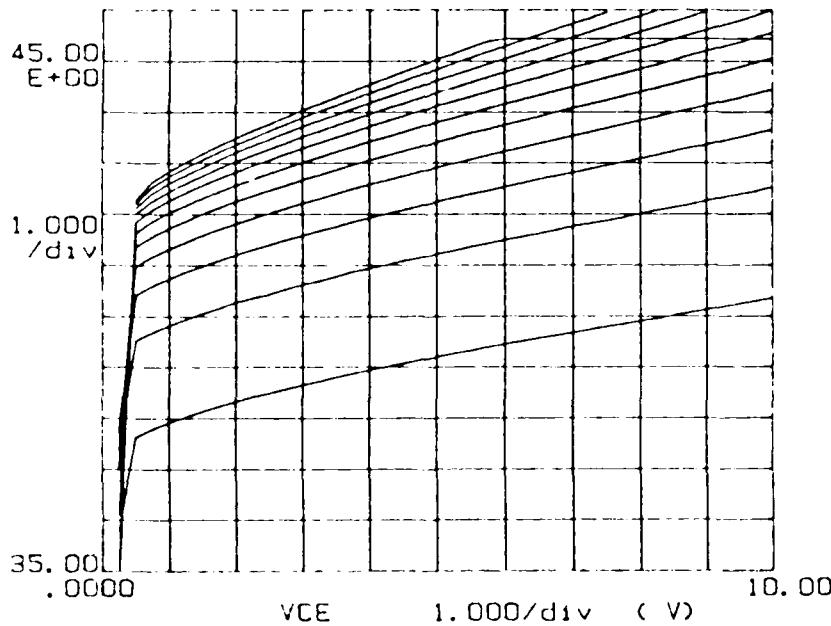
Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constant:
VE -Ch1 .0000V

$$HFE () = IC/IB$$

***** GRAPHICS PLOT *****

HFE
()



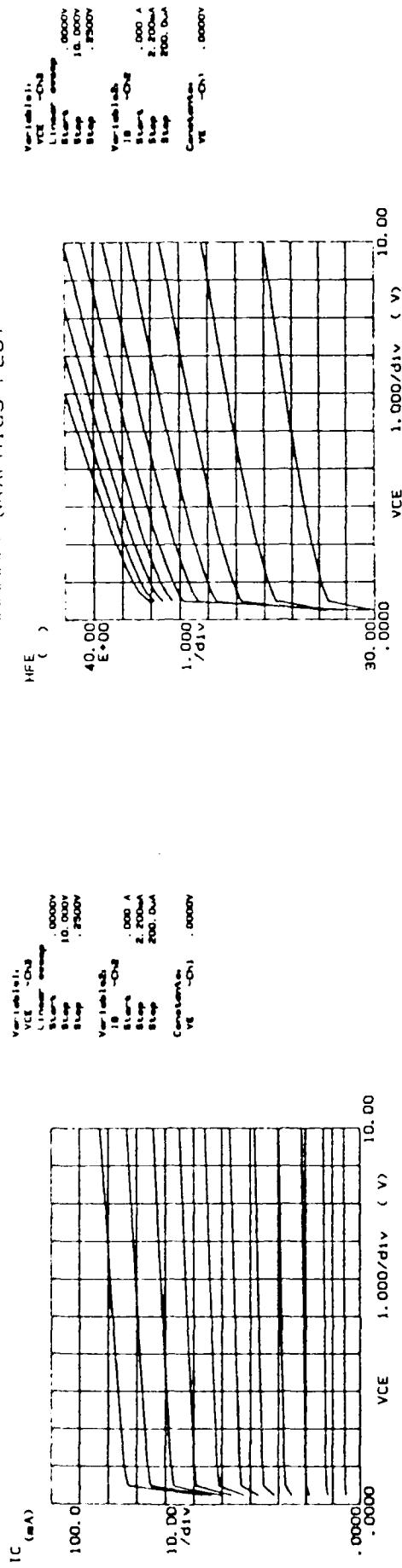
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

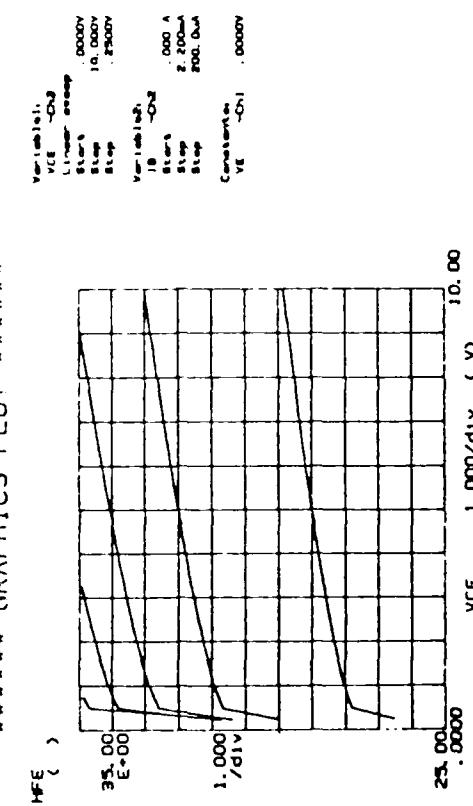
Constant:
VE -Ch1 .0000V

Figs. A.l.c

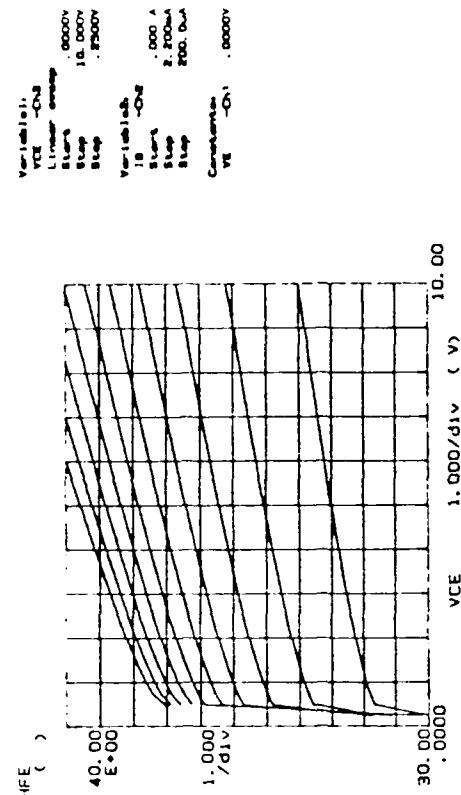
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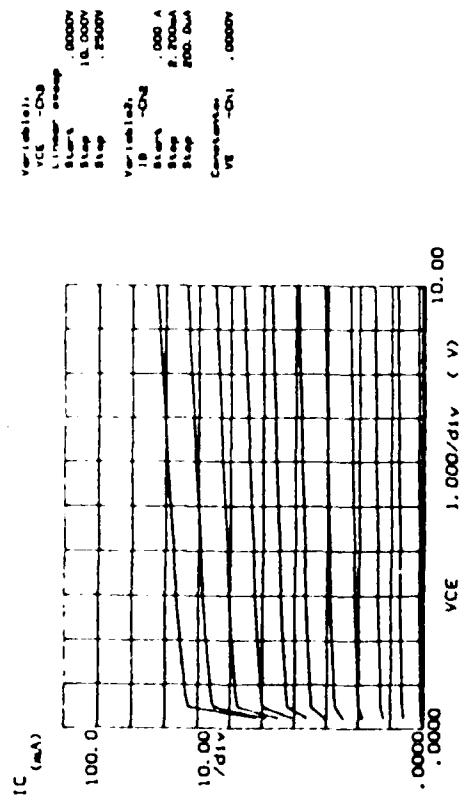


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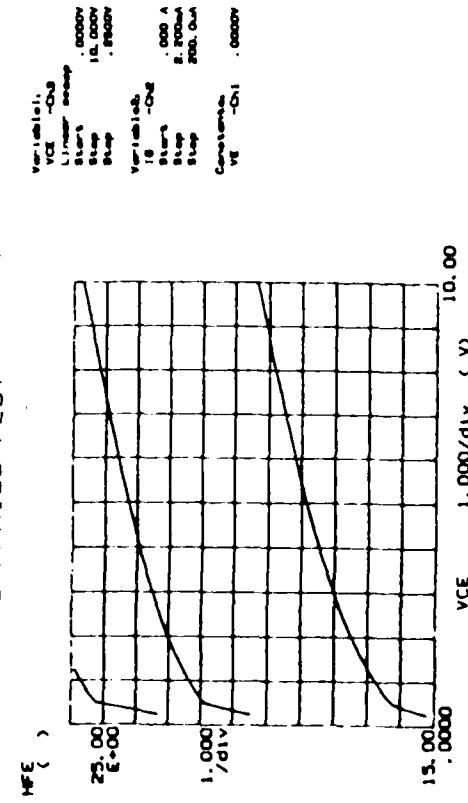


Figs. A.1.d

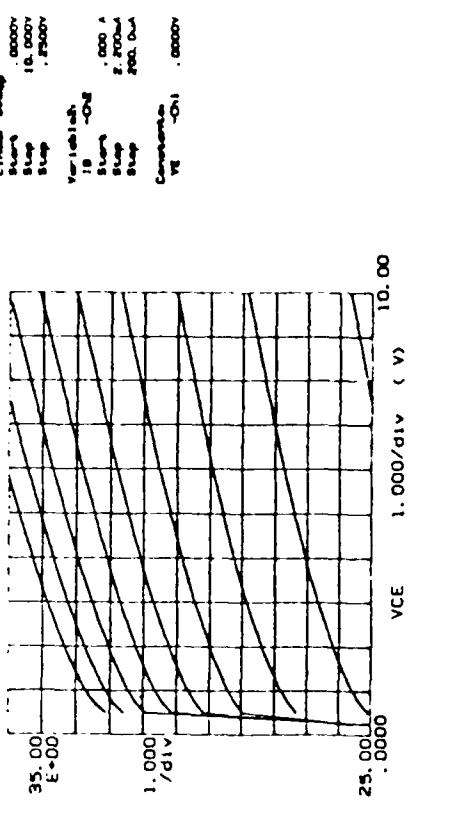
***** GRAPHICS PLOT *****



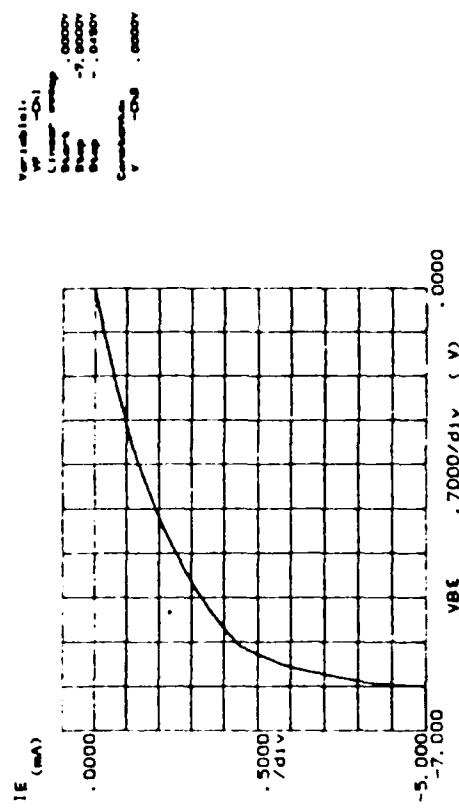
***** GRAPHICS PLOT *****



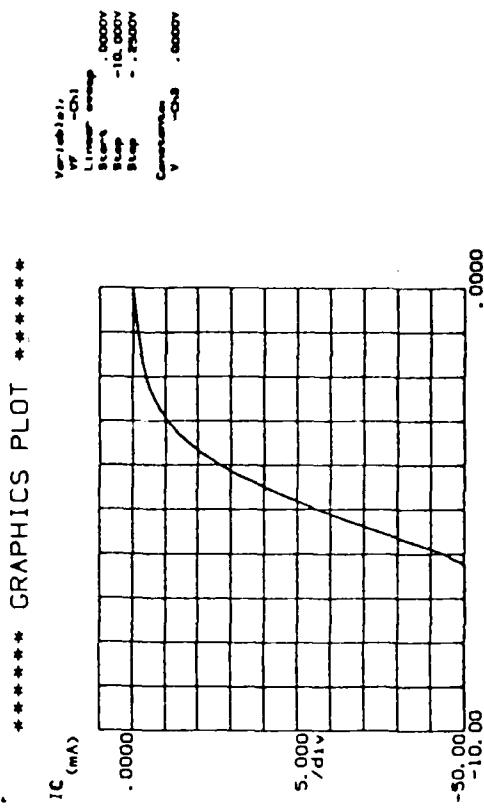
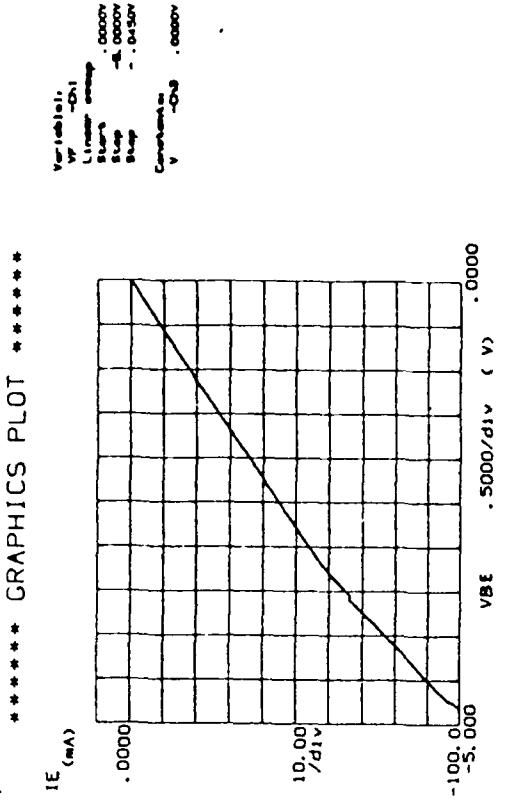
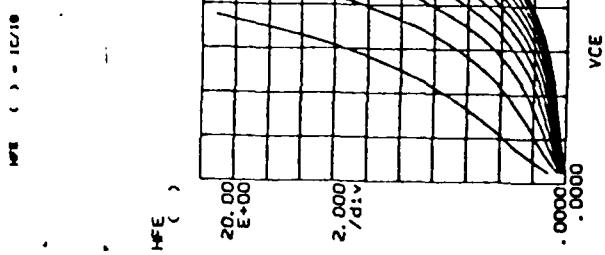
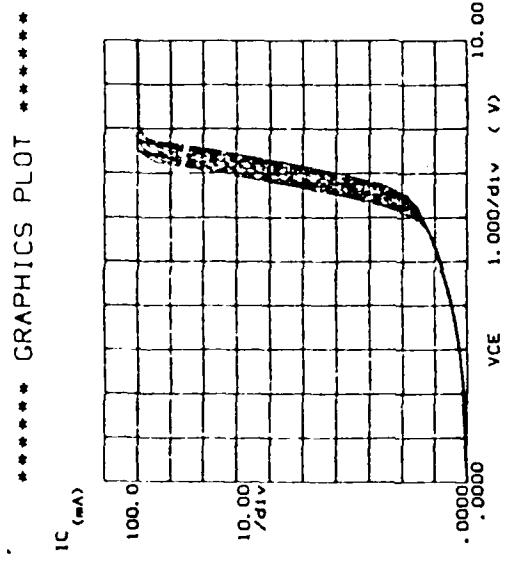
***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****

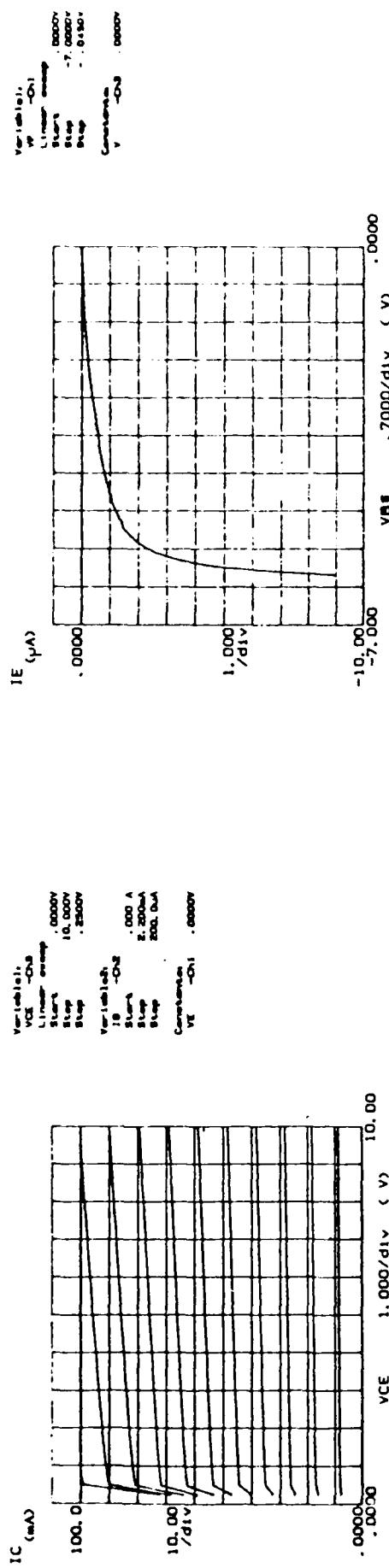


Figs. A.1.e



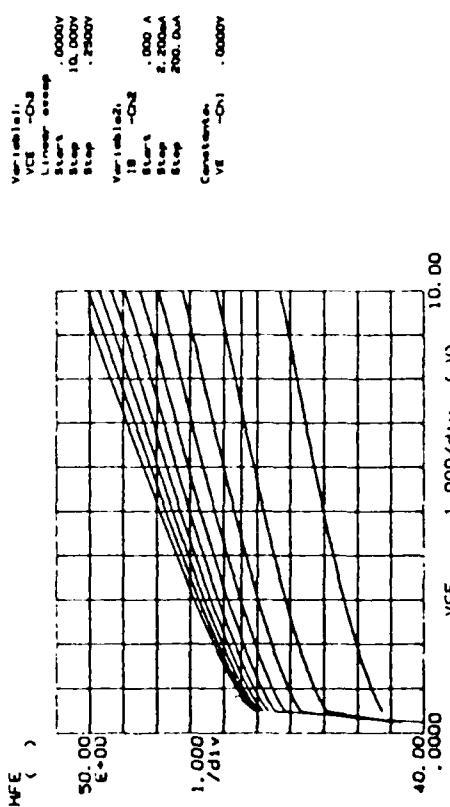
Figs. A.2.a

***** GRAPHICS PLOT *****



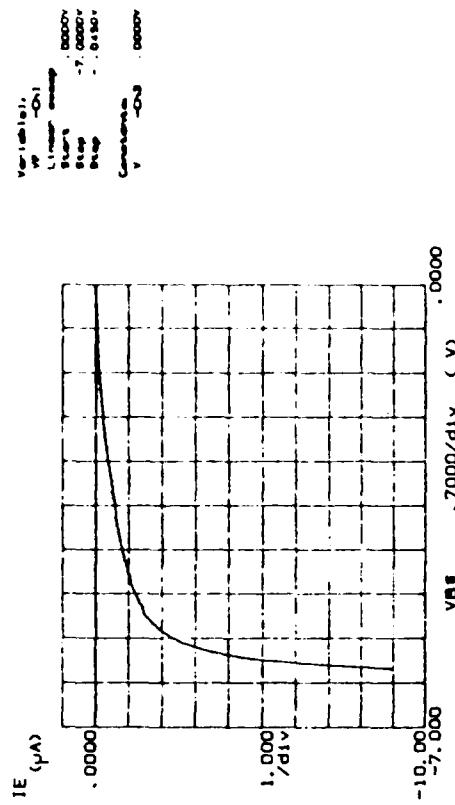
$I_C = 10 \times I_{C1}$

***** GRAPHICS PLOT *****



$H_F = 10 \times H_{F1}$

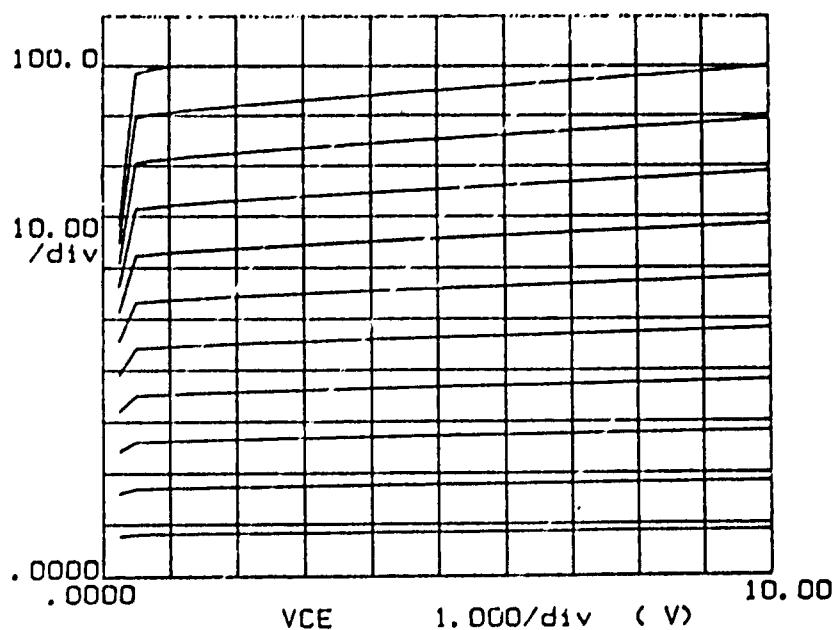
***** GRAPHICS PLOT *****



Figs. A.2.b

***** GRAPHICS PLOT *****

IC
(mA)



Variables:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

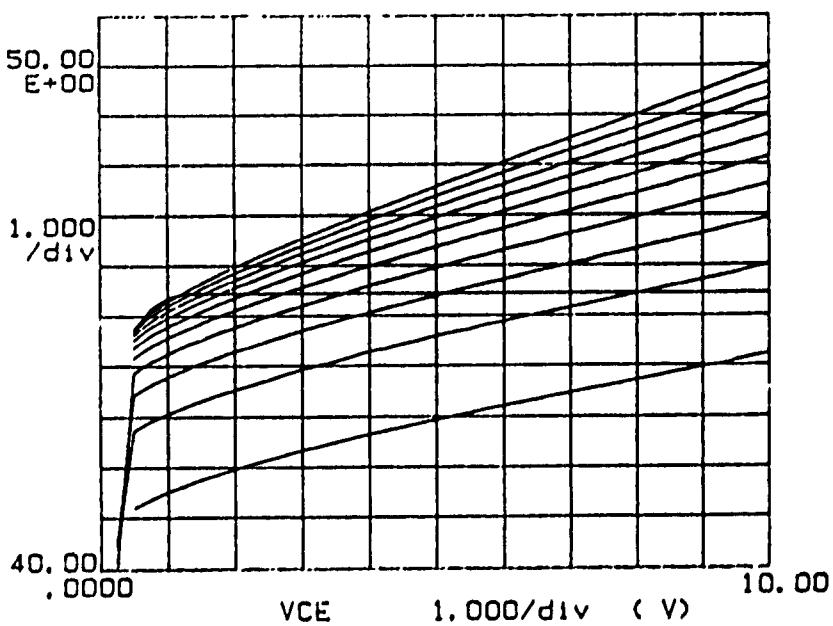
Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constant:
VE -Ch1 .0000V

$$HFE (\beta) = IC/IB$$

***** GRAPHICS PLOT *****

HFE
()

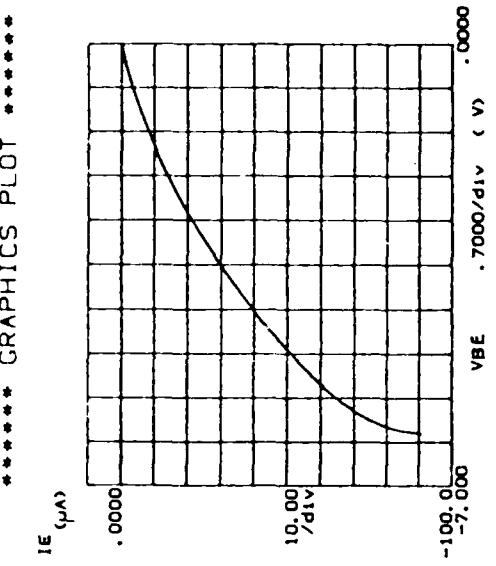
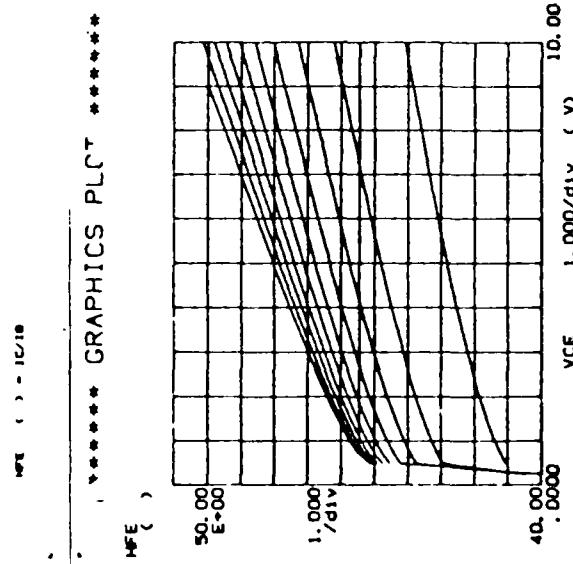
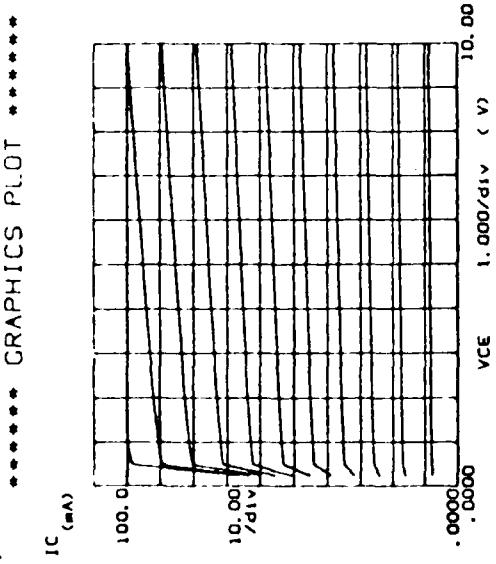


Variables:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

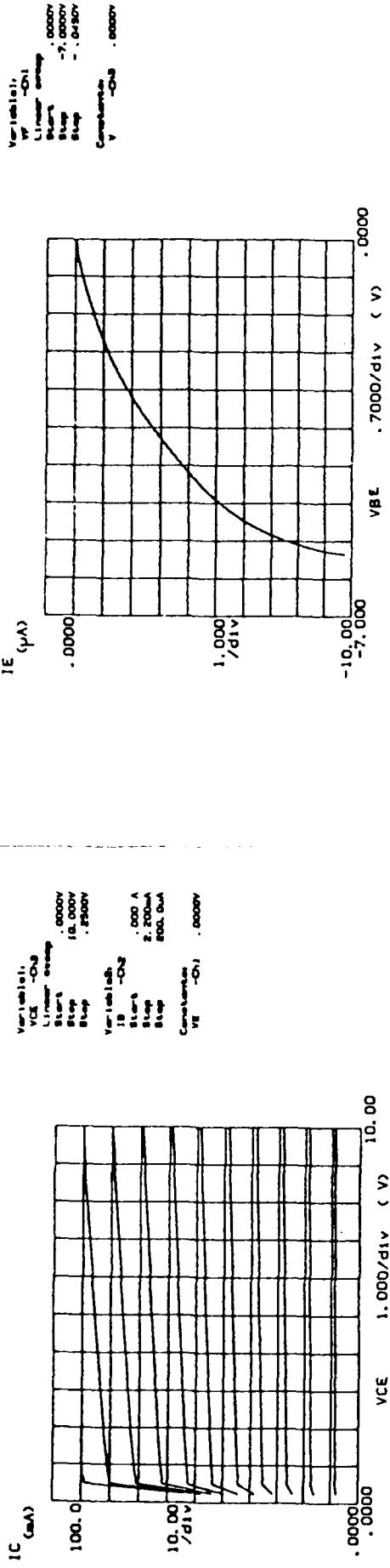
Constant:
VE -Ch1 .0000V

Figs. A.2.c

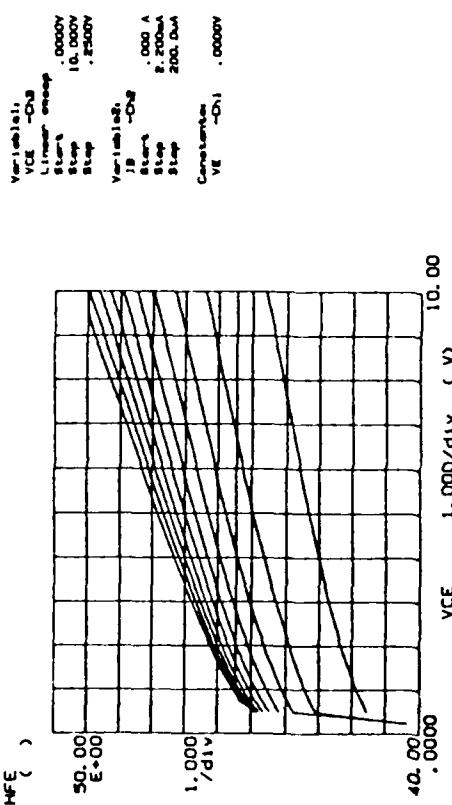


Figs. A.2.d

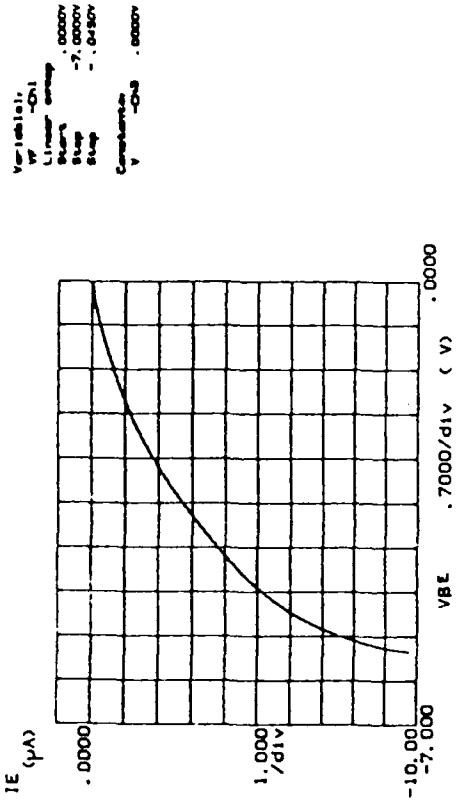
***** GRAPHICS PLOT *****



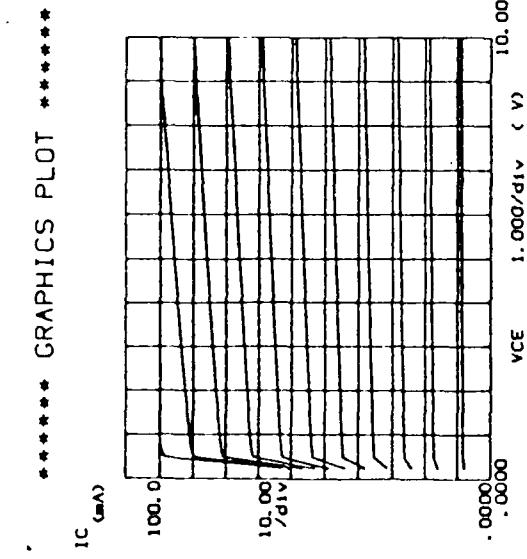
***** GRAPHICS PLOT *****



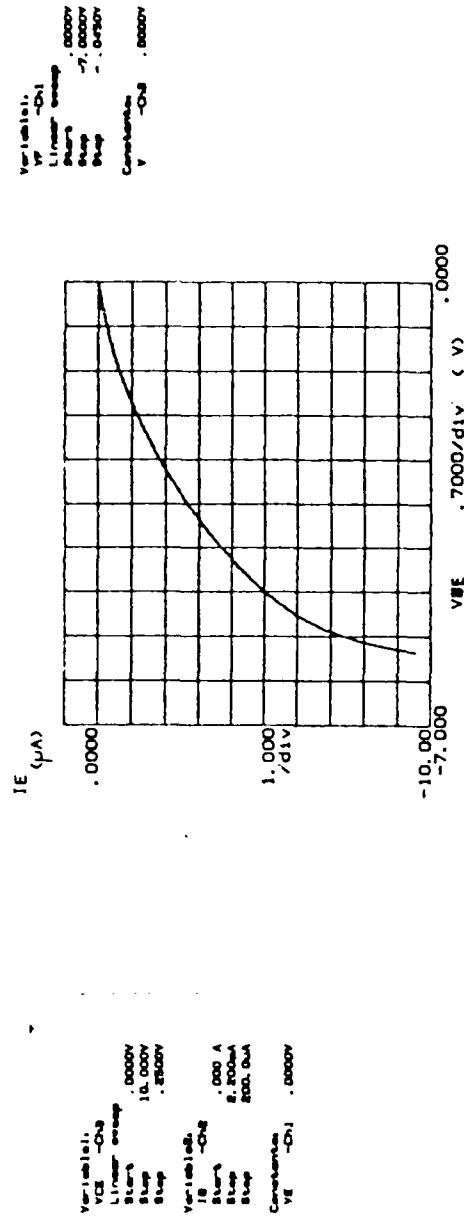
***** GRAPHICS PLOT *****



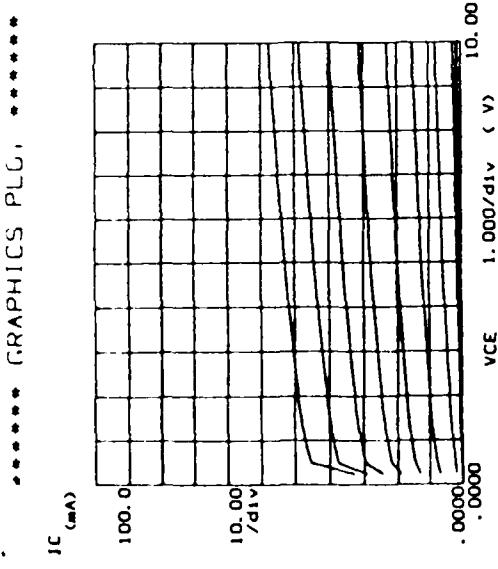
Figs. A.2.e



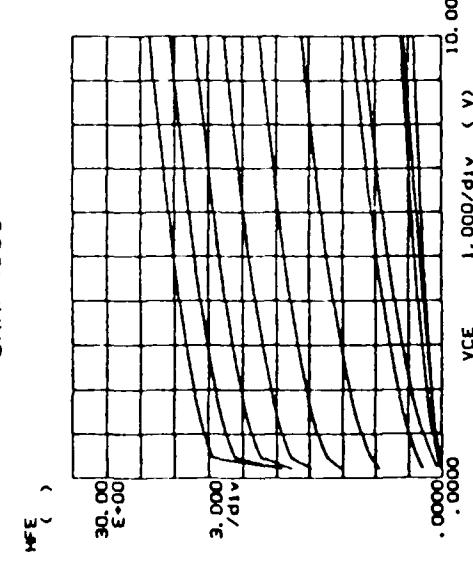
- 38 -



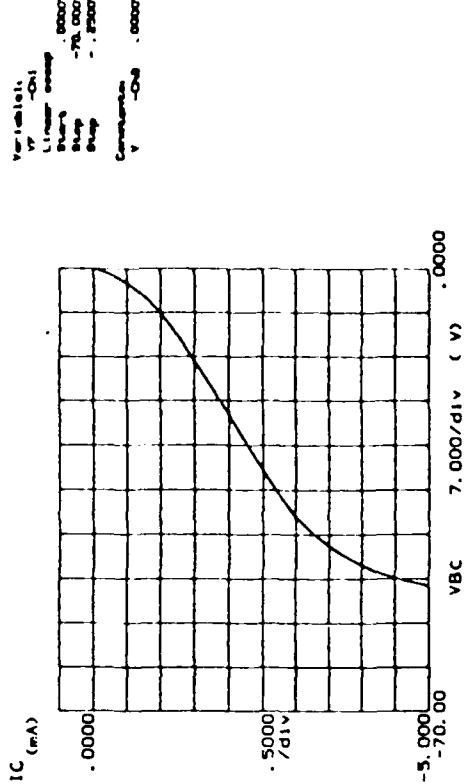
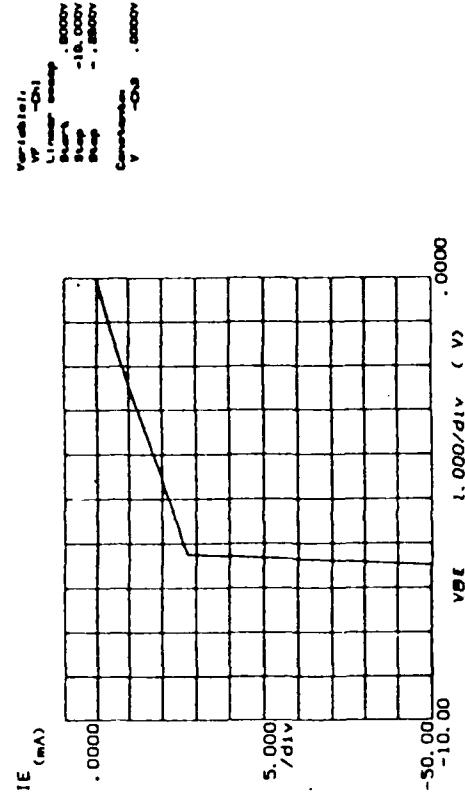
Figs. A.2.f



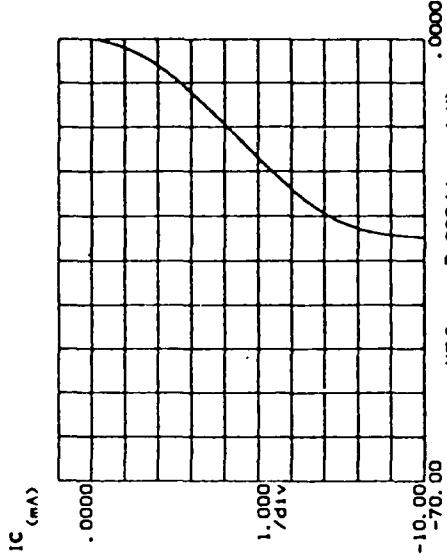
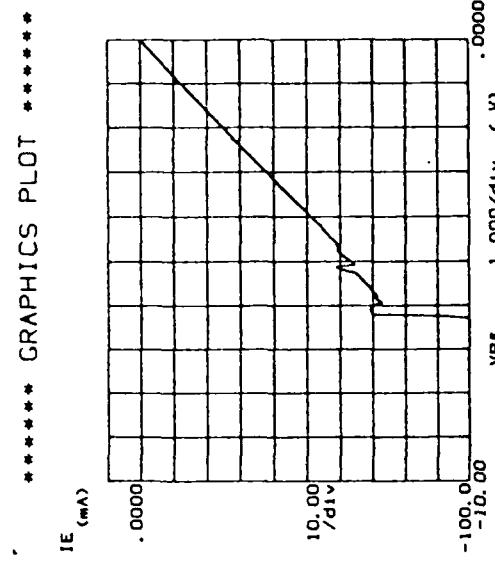
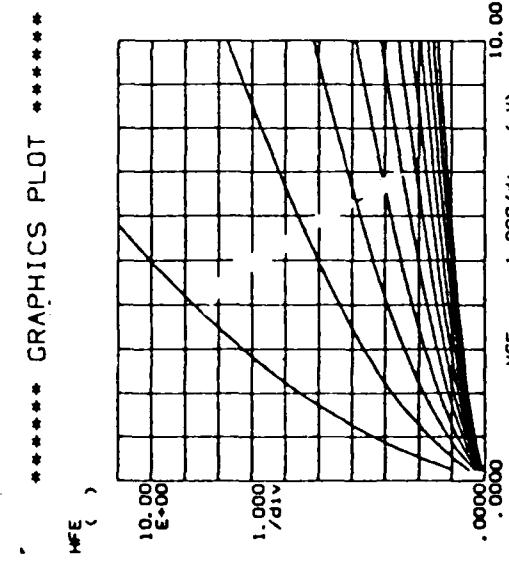
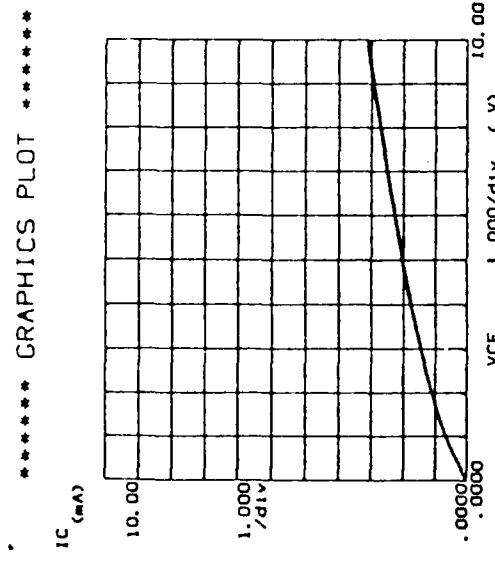
IB = 1e-10



IB = 1e-10



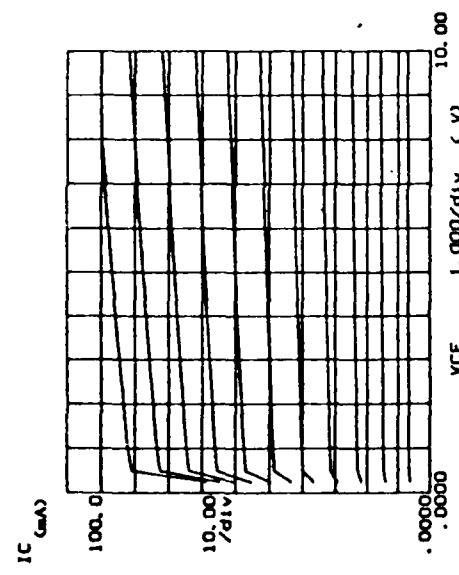
Figs. A.2.g



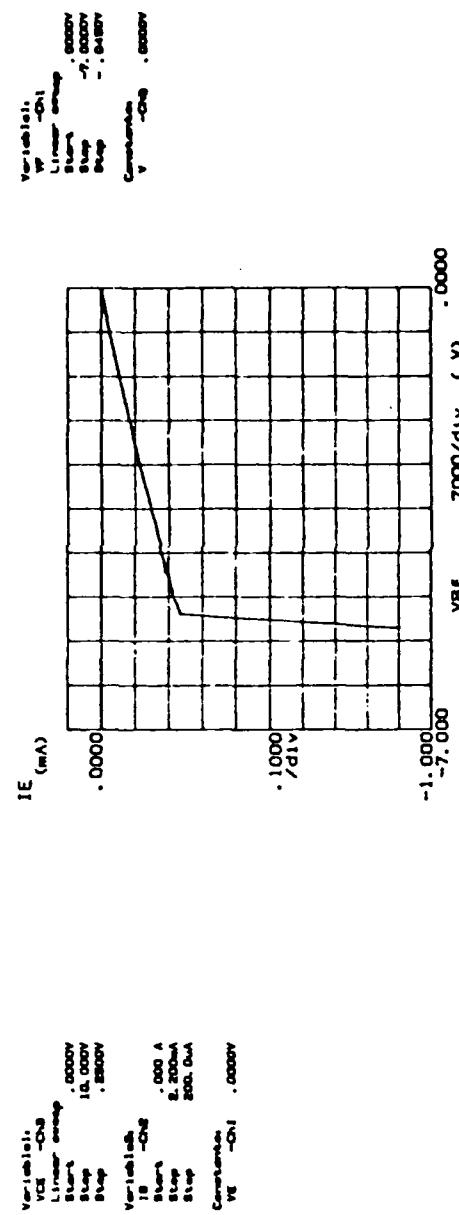
ME 1.0 - 10/10

Figs. A.3.a

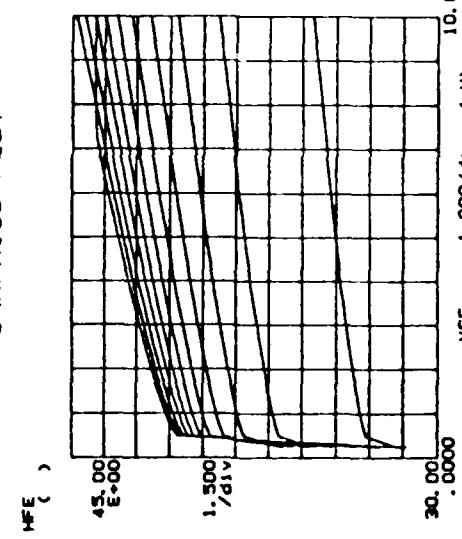
***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****

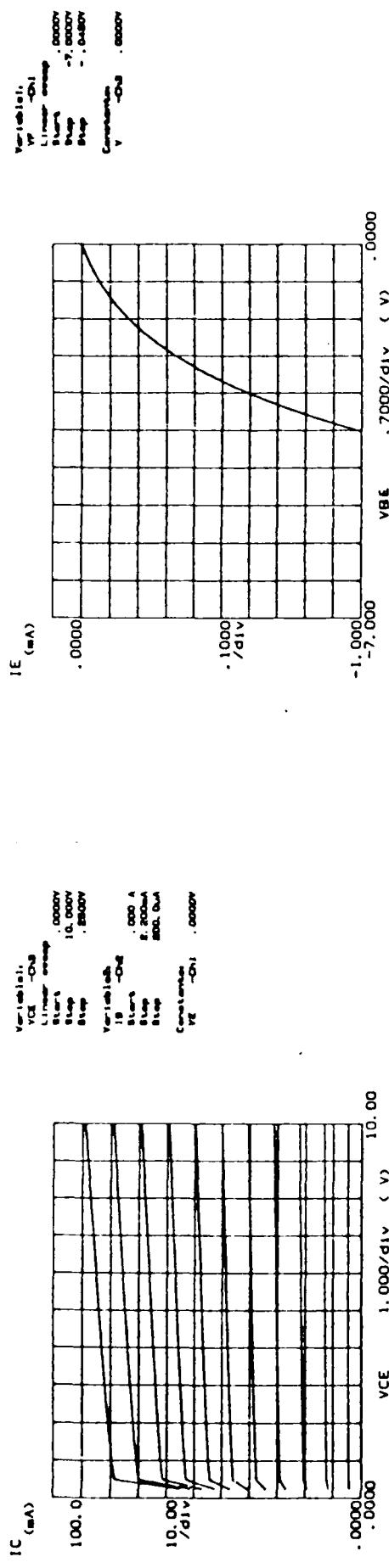


***** GRAPHICS PLOT *****



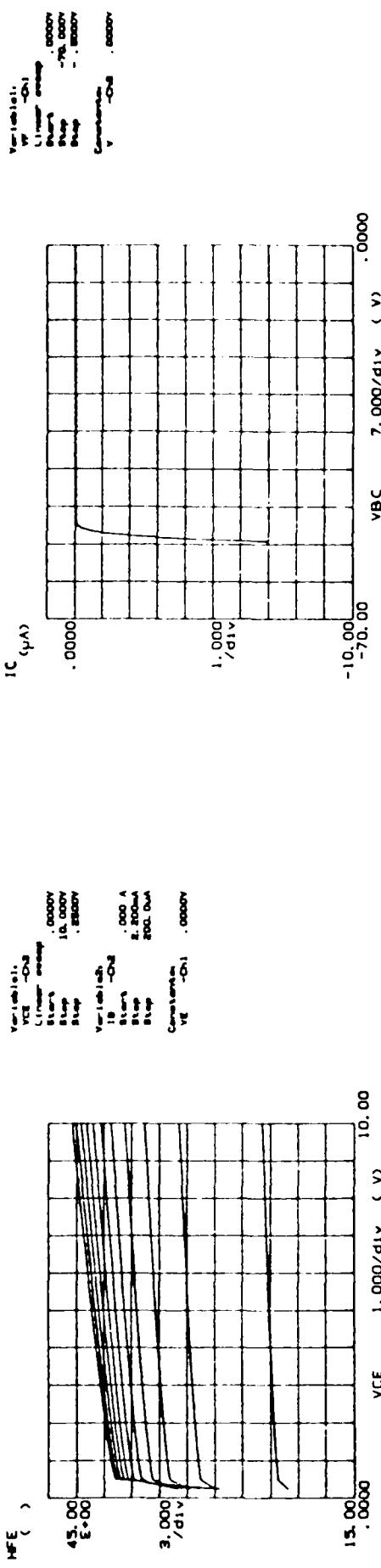
Figs. A.3.b

***** GRAPHICS PLOT *****



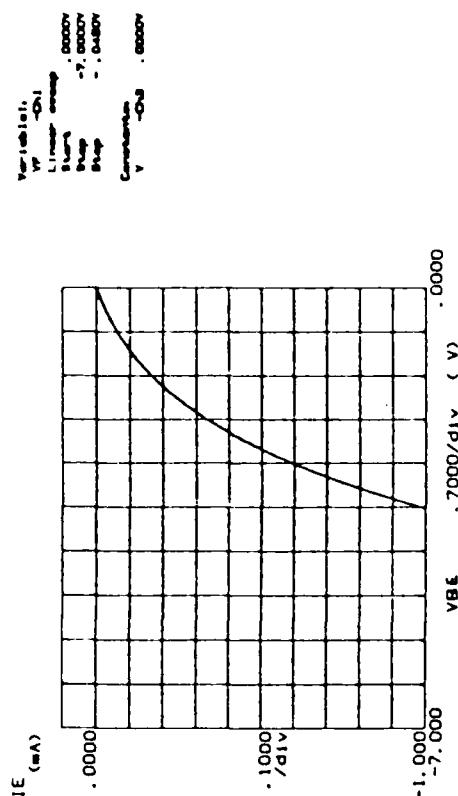
NOTE: $\downarrow \rightarrow I_C/10$

***** GRAPHICS PLOT *****

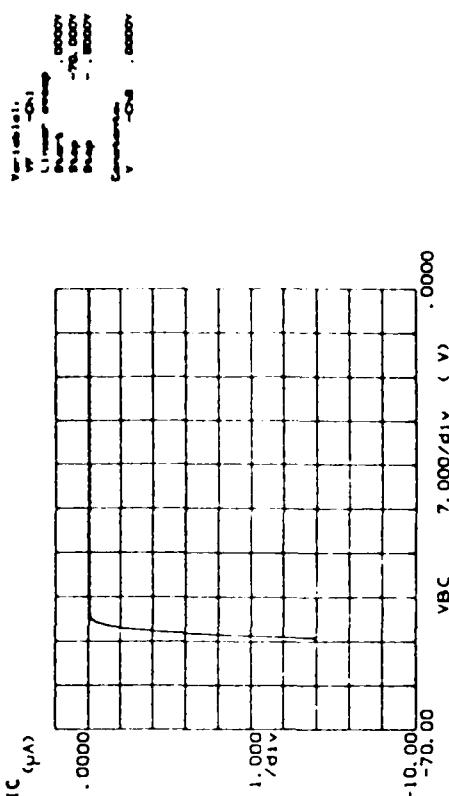


NOTE: $\downarrow \rightarrow I_C/10$

***** GRAPHICS PLOT *****

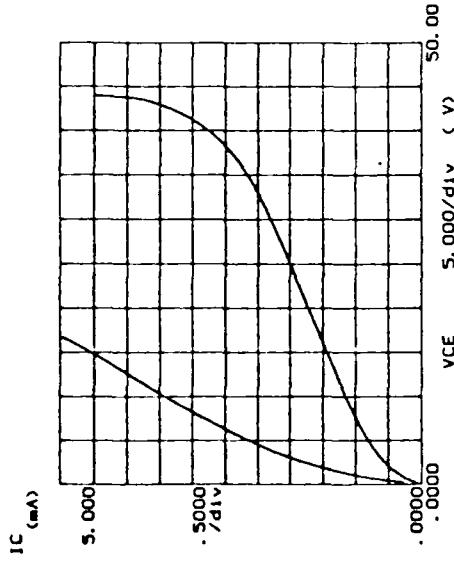


***** GRAPHICS PLOT *****

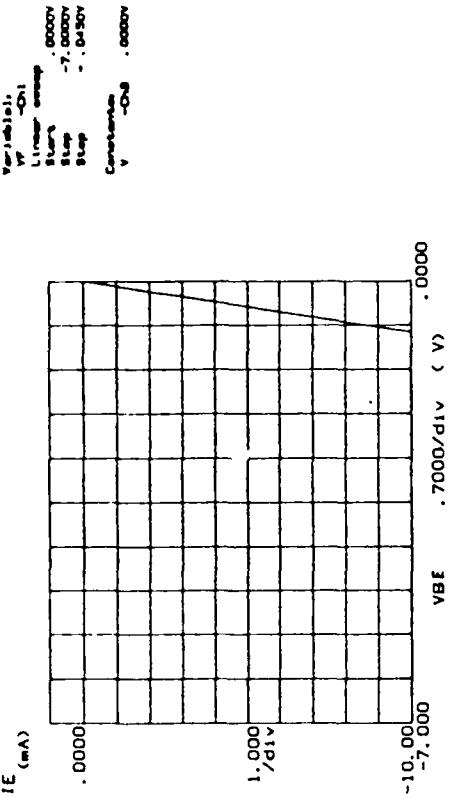


Figs. A.3.c

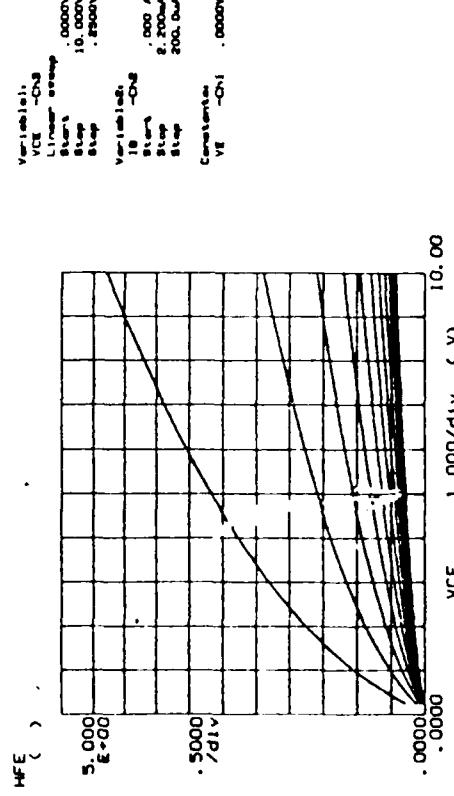
***** GRAPHICS PLOT *****



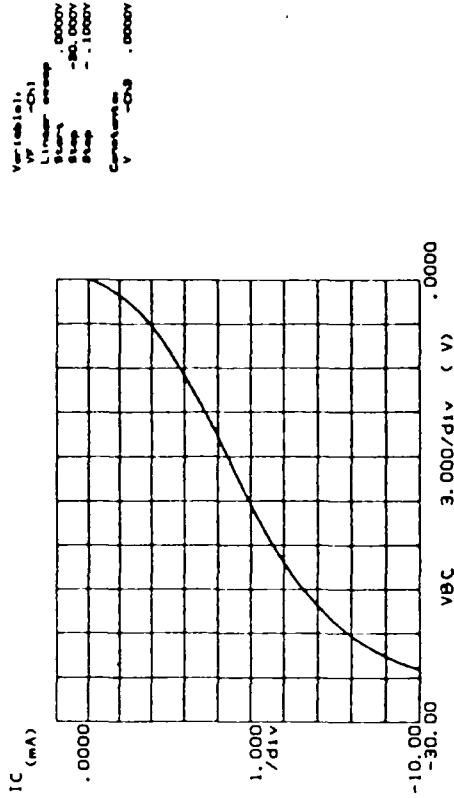
***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****

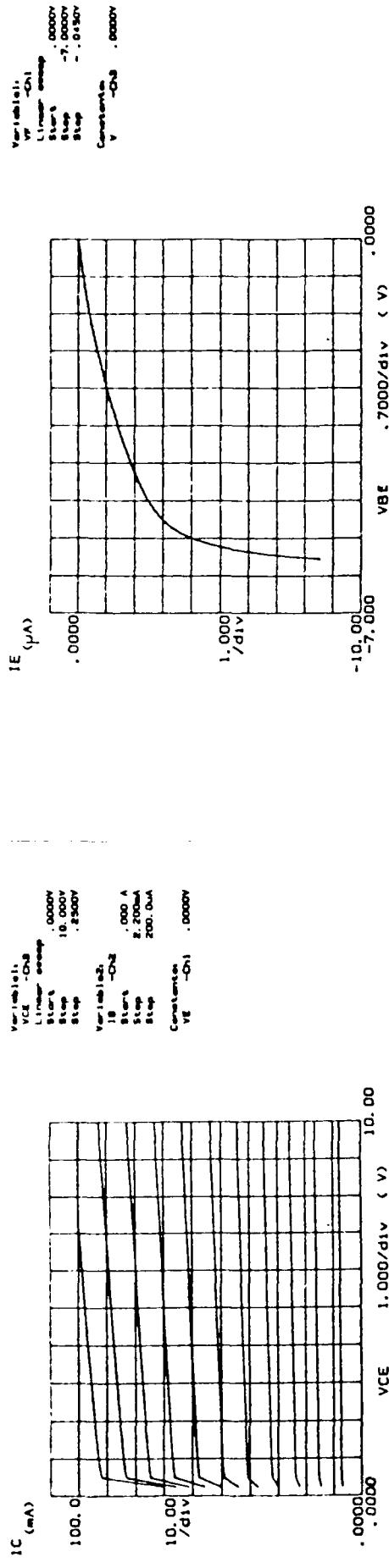


***** GRAPHICS PLOT *****

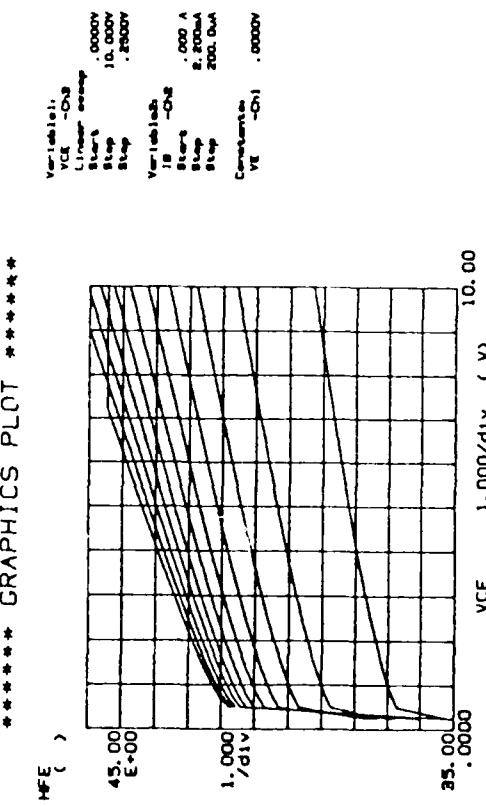


Figs. A.4.a

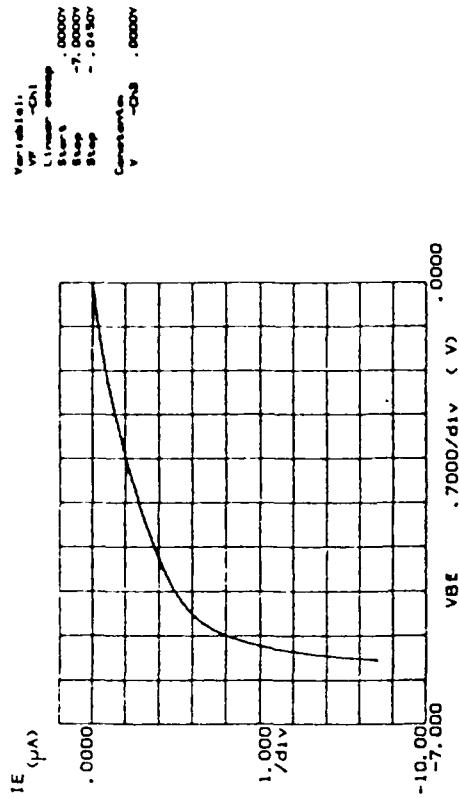
***** GRAPHICS PLOT *****



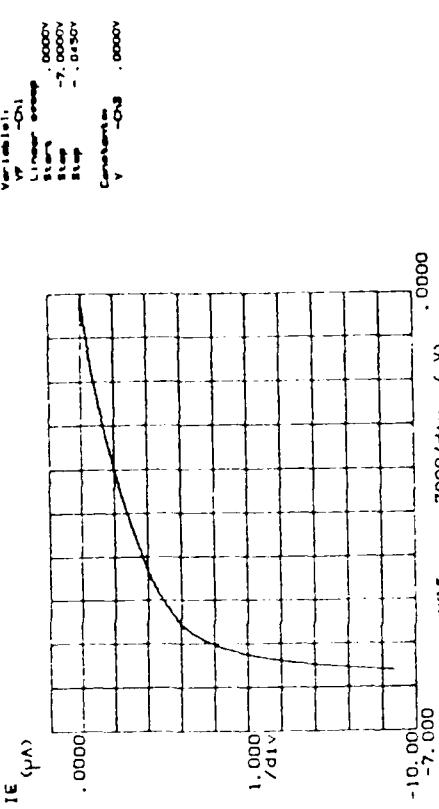
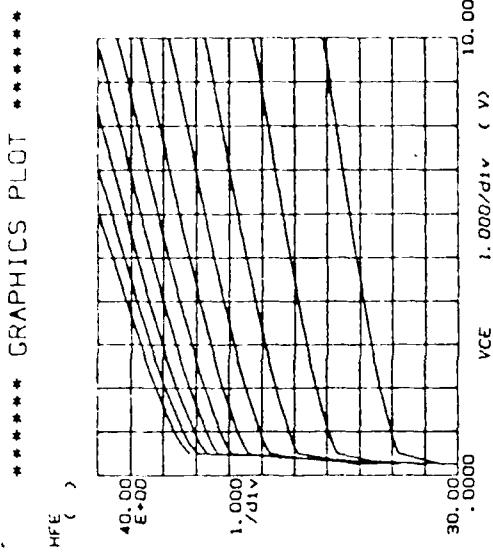
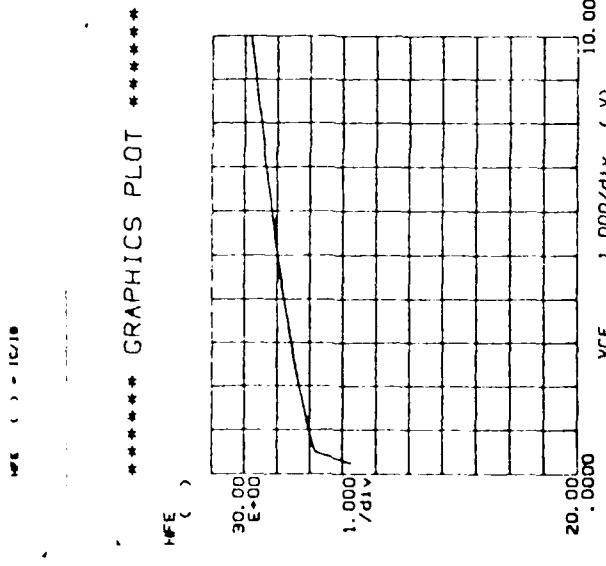
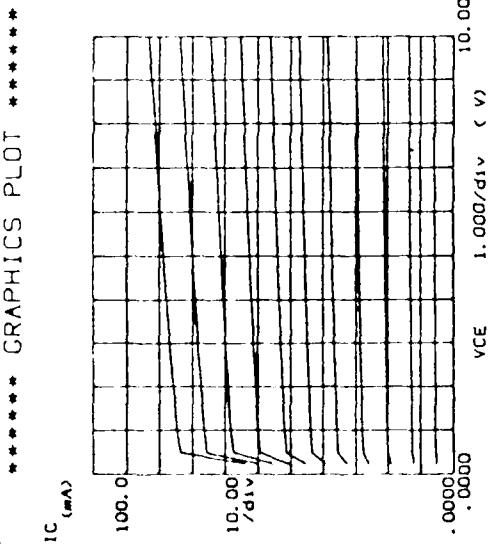
***** GRAPHICS PLOT *****



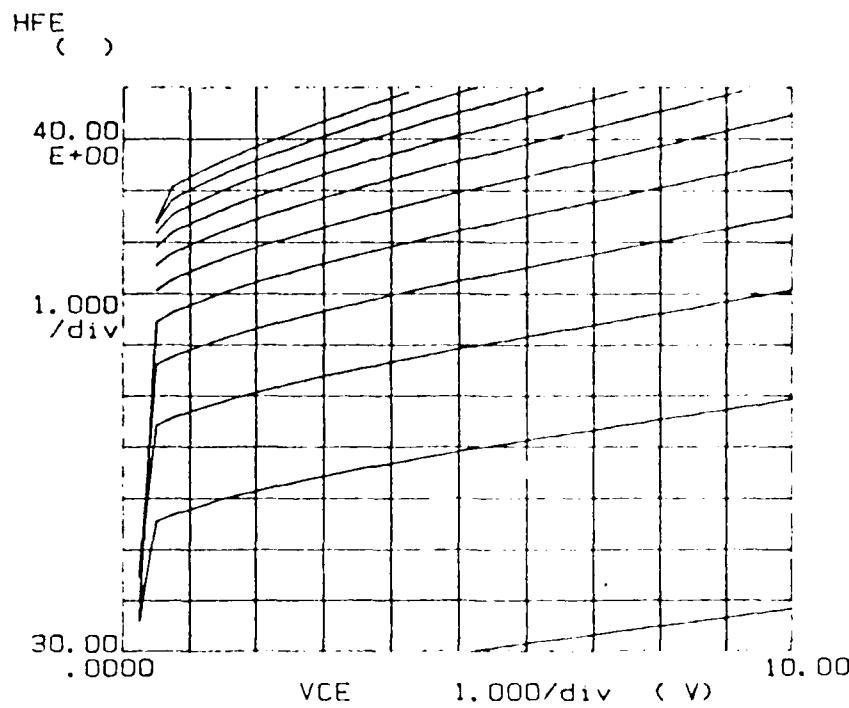
***** GRAPHICS PLOT *****



Figs. A.4.c



Figs. A.4.d



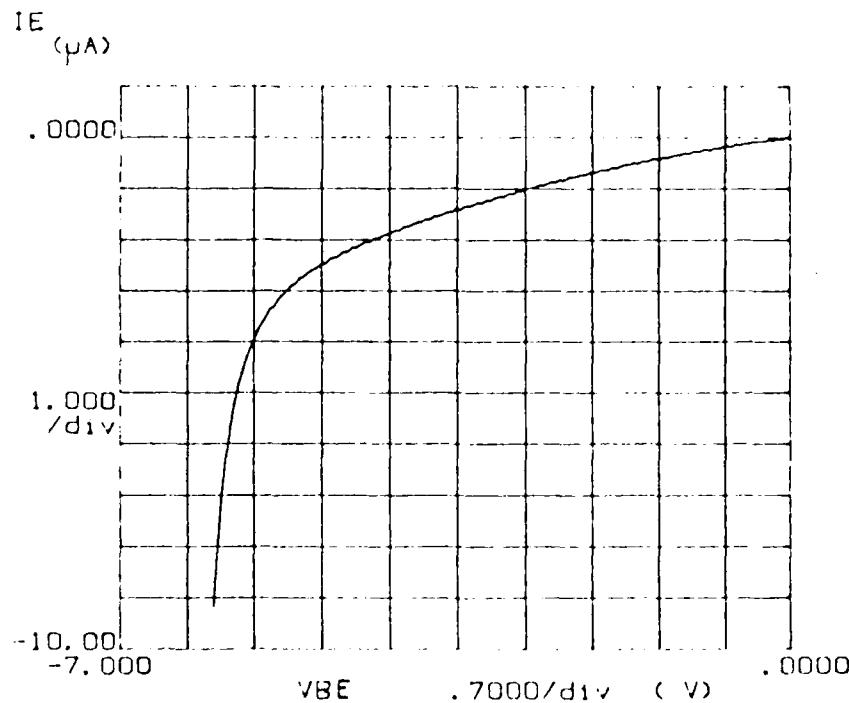
Variables:
 VCE -Ch3
 Linear sweep
 Start .0000V
 Stop 10.000V
 Step .2500V

Variables2:
 IB -Ch2
 Start .000 A
 Stop 2.200mA
 Step 200.0uA

Constant:
 VE -Ch1 .0000V

$$HFE () = IC/IB$$

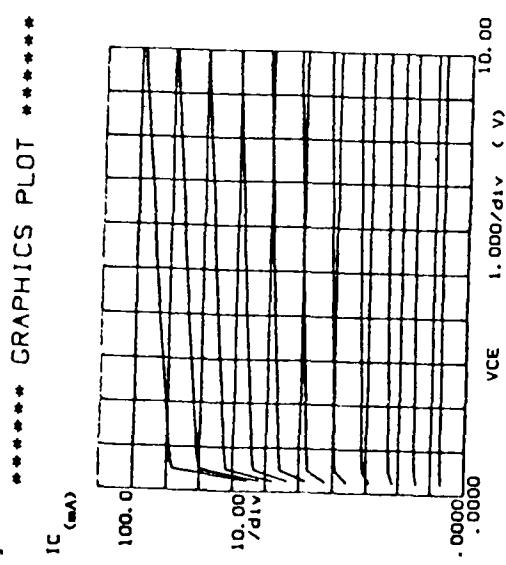
***** GRAPHICS PRINT *****



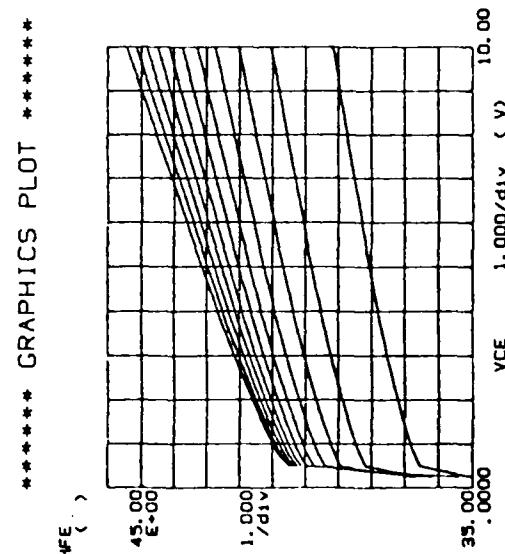
Variables:
 VF -Ch1
 Linear sweep
 Start .0000V
 Stop -7.0000V
 Step -.0450V

Constant:
 V -Ch3 .0000V

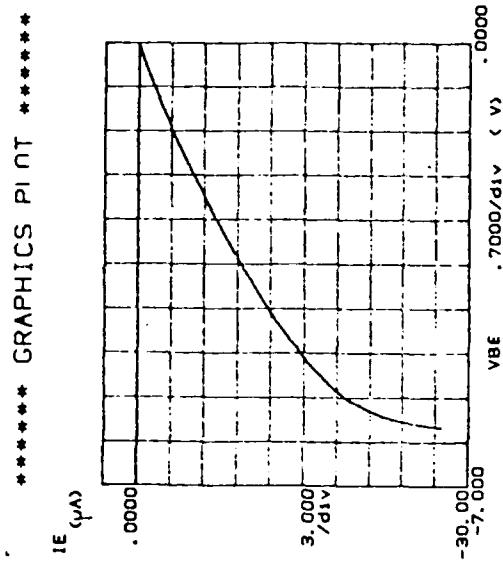
Figs. A.5.a



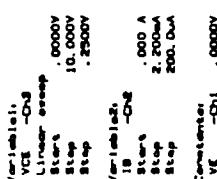
NOTE: $\downarrow \rightarrow$ IC/10



NOTE: $\downarrow \rightarrow$ IC/10



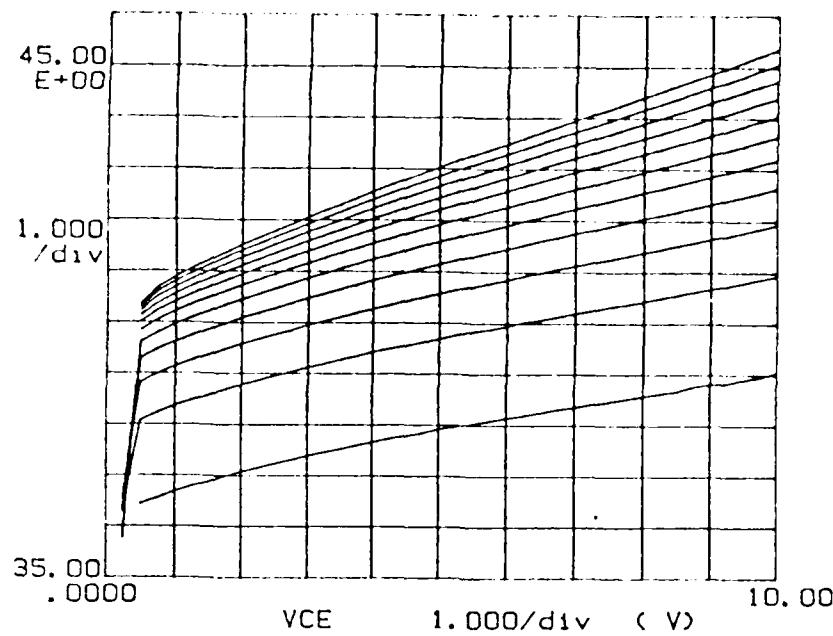
NOTE: $\downarrow \rightarrow$ IC/10



Figs. A.5.b

***** GRAPHICS PLOT *****

HFE
()



Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

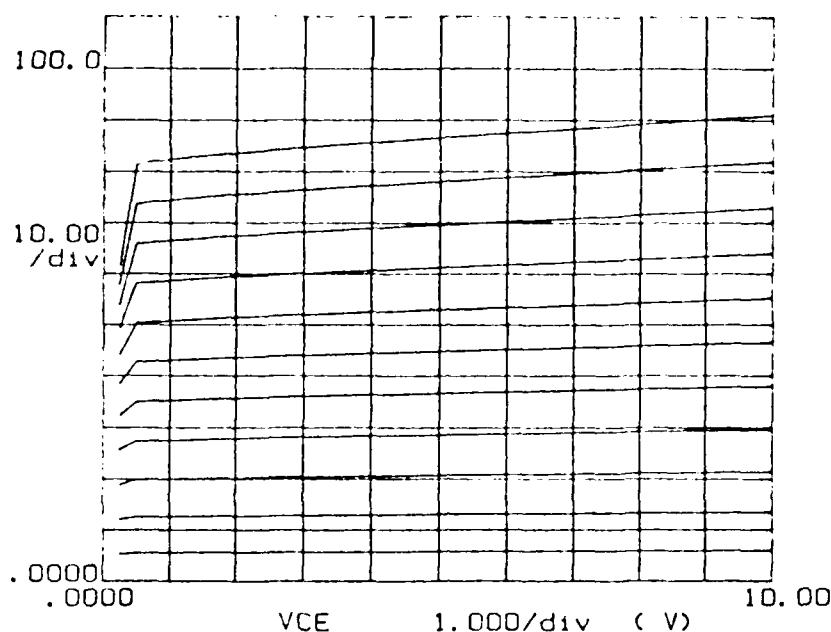
Constant:
VE -Ch1 .0000V

HFE () = IC/IB

Figs. A.5.c

***** GRAPHICS PLOT *****

IC
(mA)



Variables:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

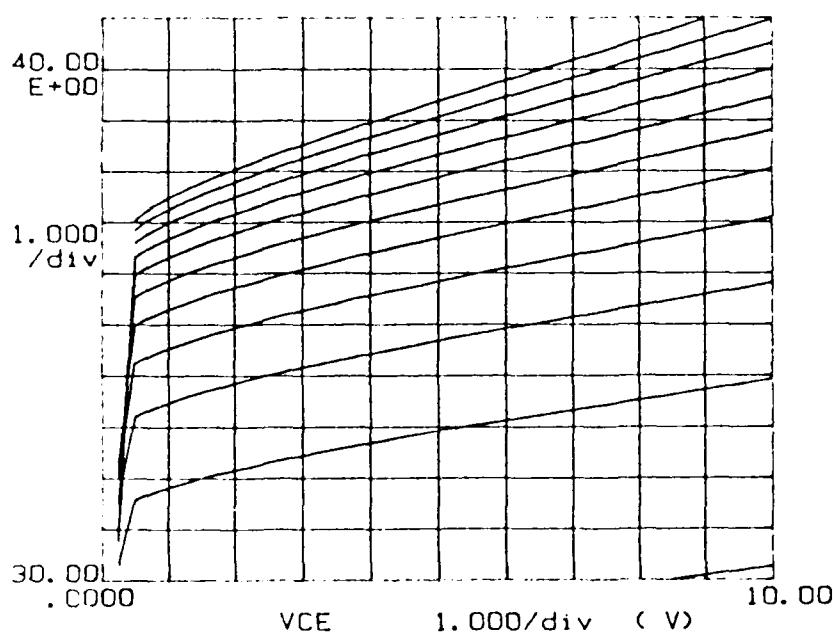
Variables2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE () = IC/IB

***** GRAPHICS PLOT *****

HFE
()



Variables:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

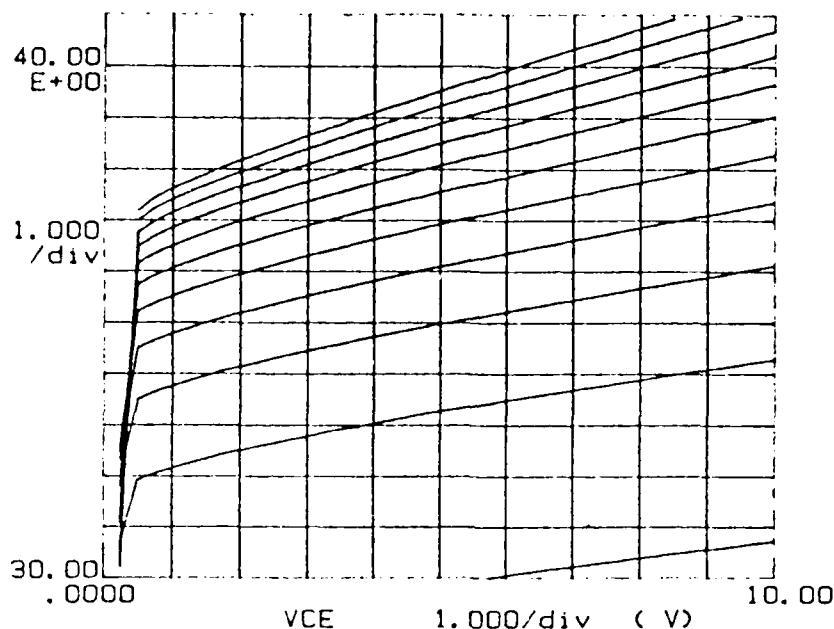
Variables2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

Figs. A.5.d

***** GRAPHICS PLOT *****

HFE
()



Variables:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

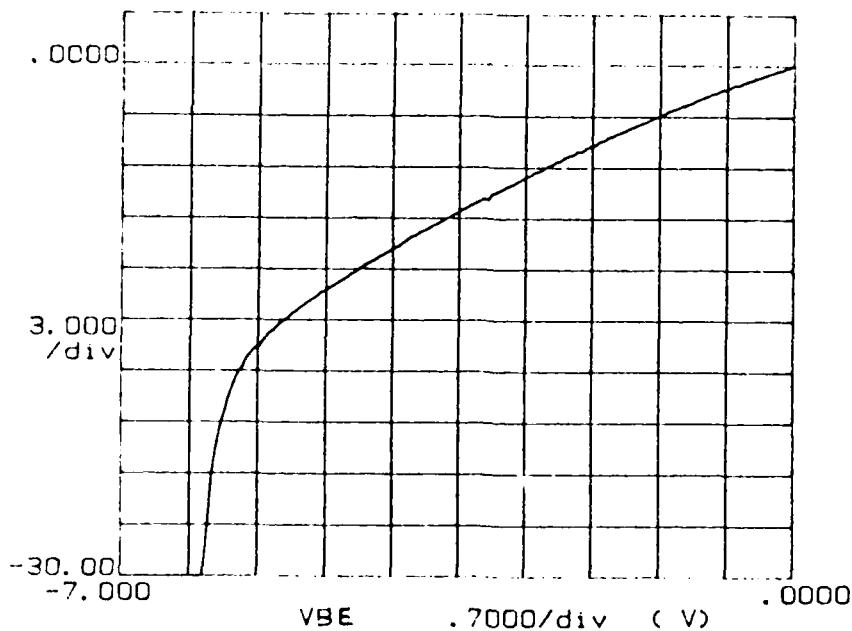
Variables2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE () = IC/IB

***** GRAPHICS PLOT *****

IE
(μ A)



Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop -7.0000V
Step -.0450V

Constants:
V -Ch3 .0000V

Figs. B.1.a

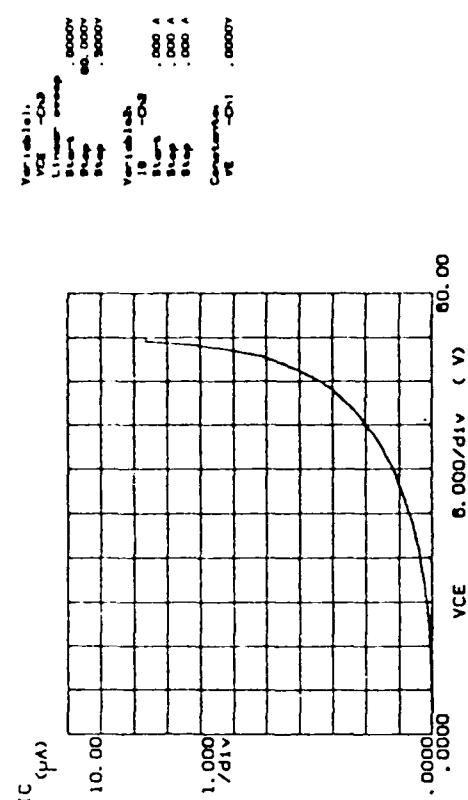
***** GRAPHICS PLOT *****



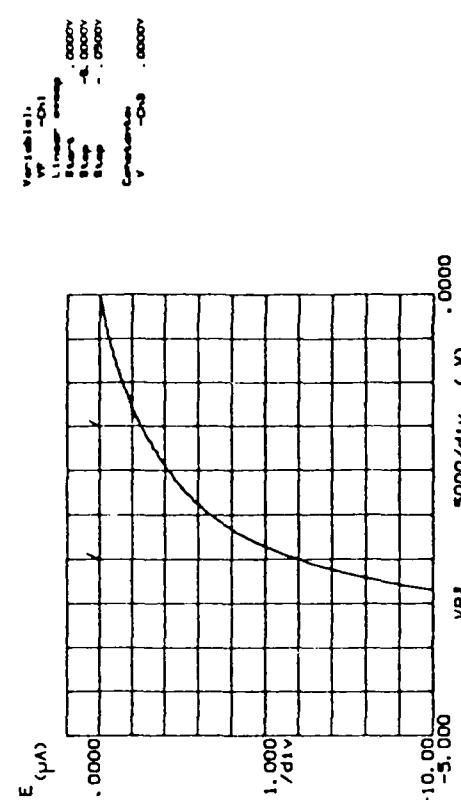
***** GRAPHICS PLL *****



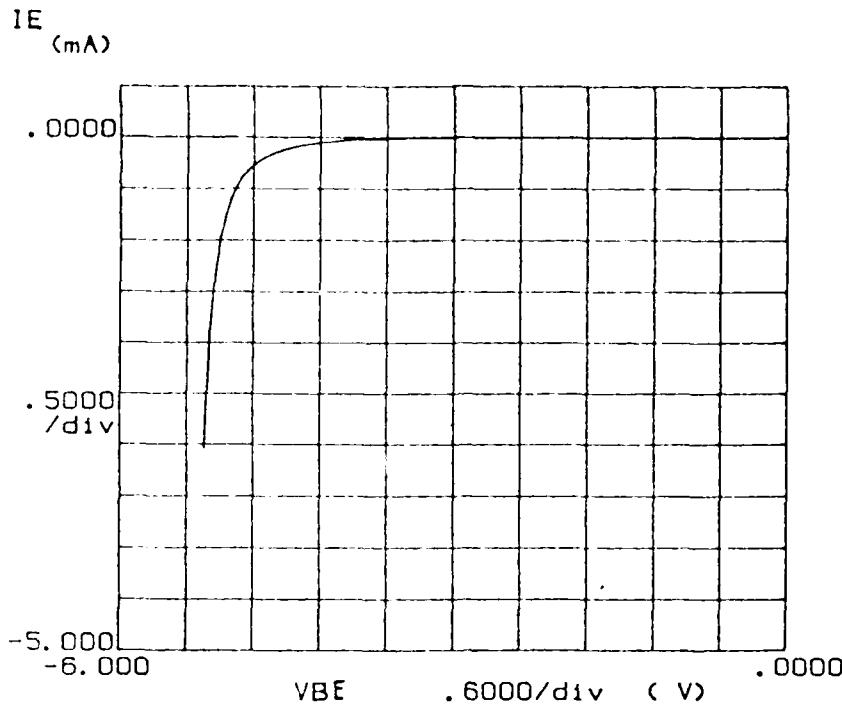
***** GRAPHICS PI *****



***** GRAPHICS PLU *****



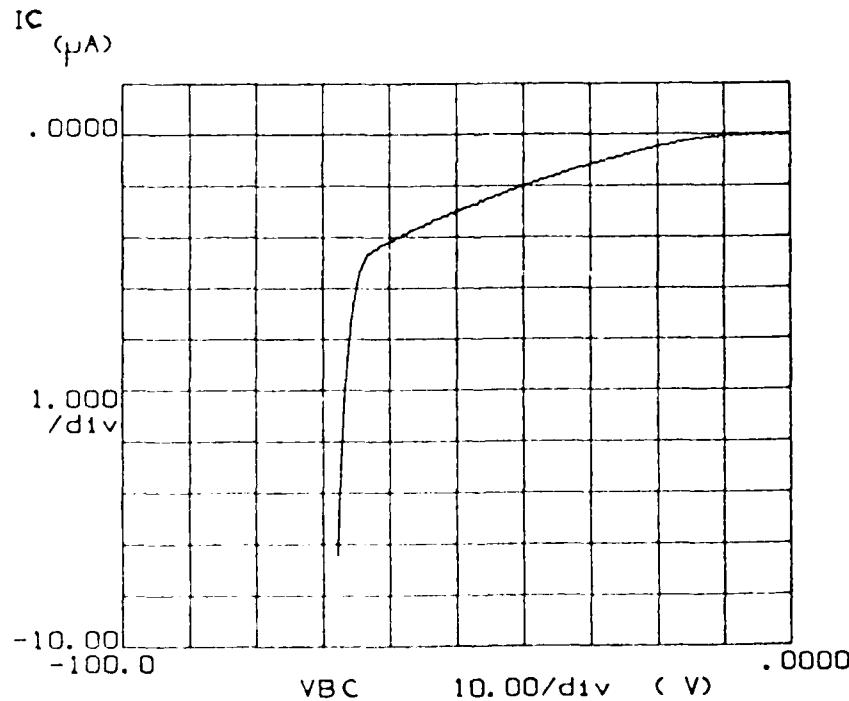
***** GRAPHICS PLOT *****



Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop -8.0000V
Step -.0500V

Constants:
V -Ch3 .0000V

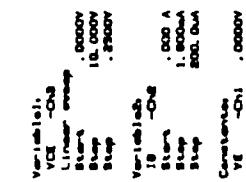
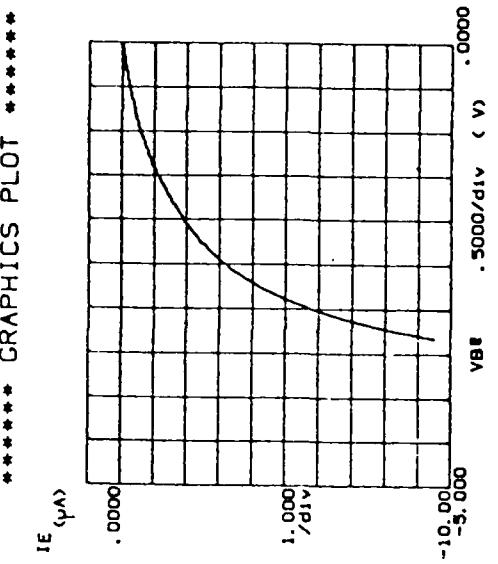
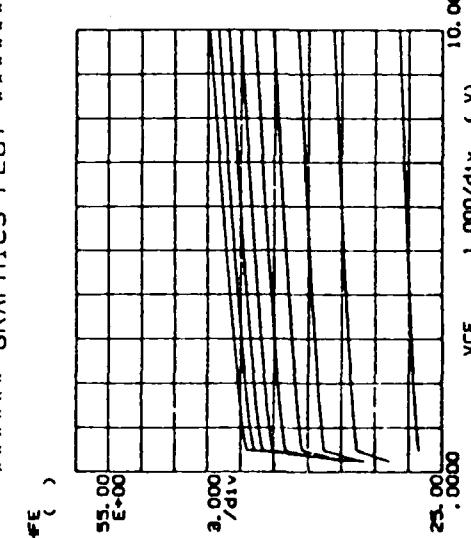
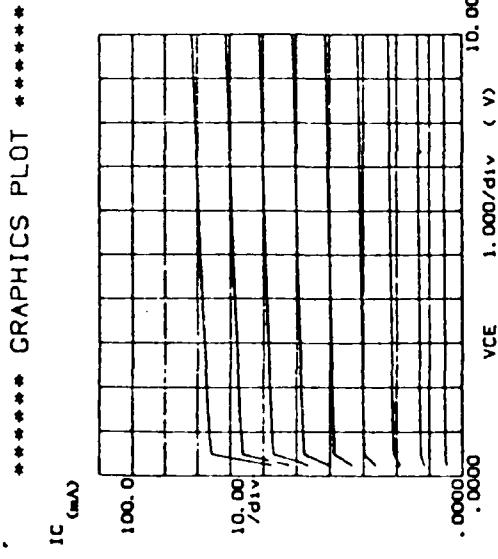
***** GRAPHICS PLC *****



Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop -100.00V
Step -.5000V

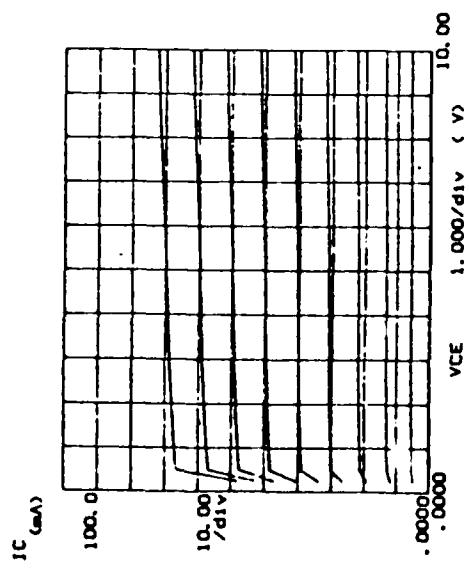
Constants:
V -Ch3 .0000V

Figs. B.1.b

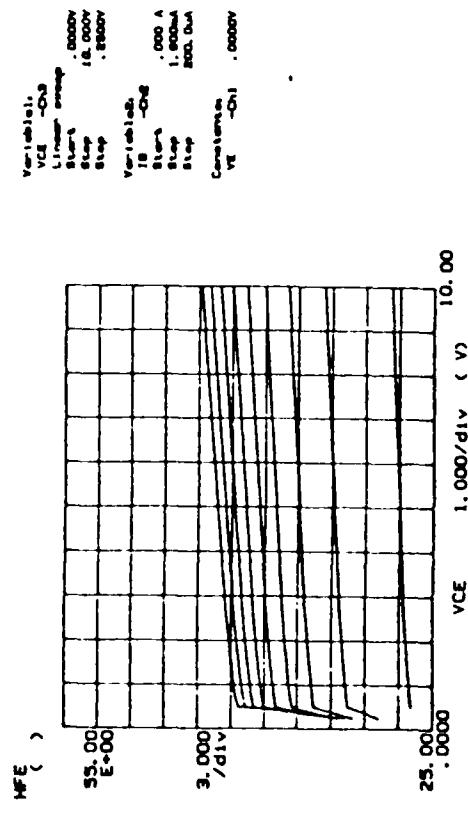


Figs. B.1.c

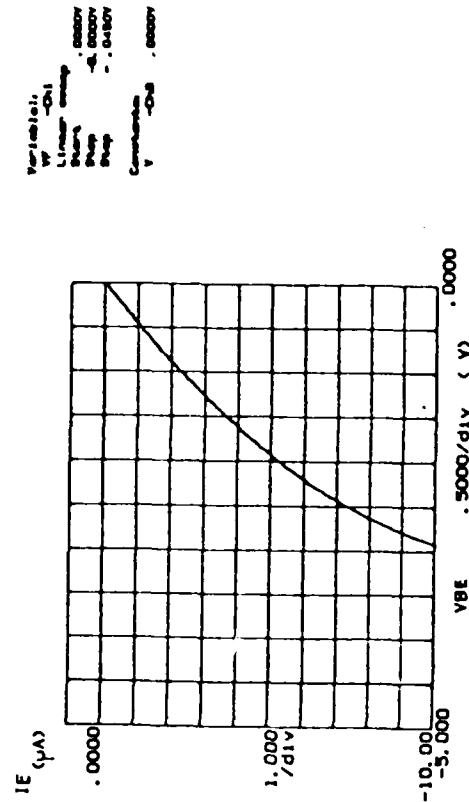
***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****

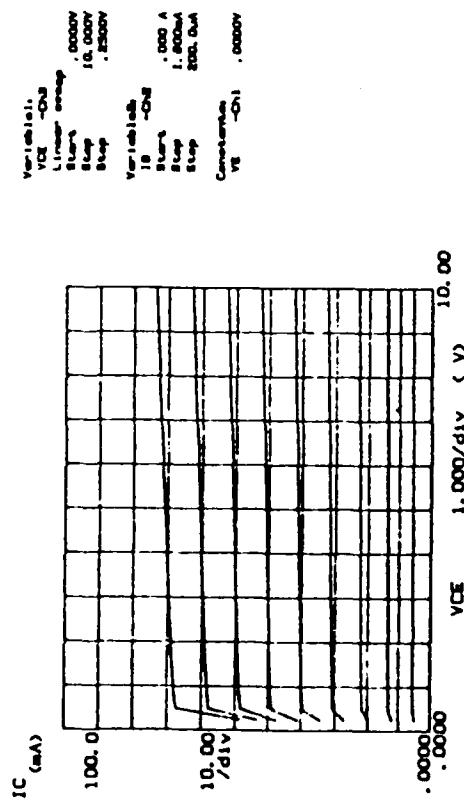


***** GRAPHICS PLOT *****

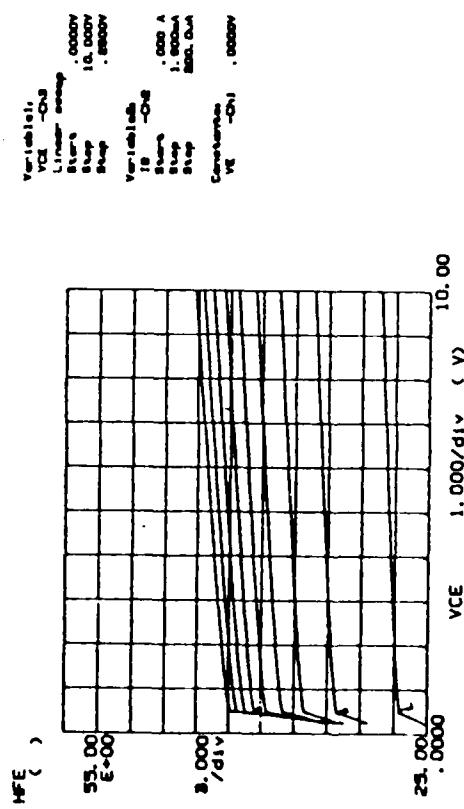


Figs. B.1.d

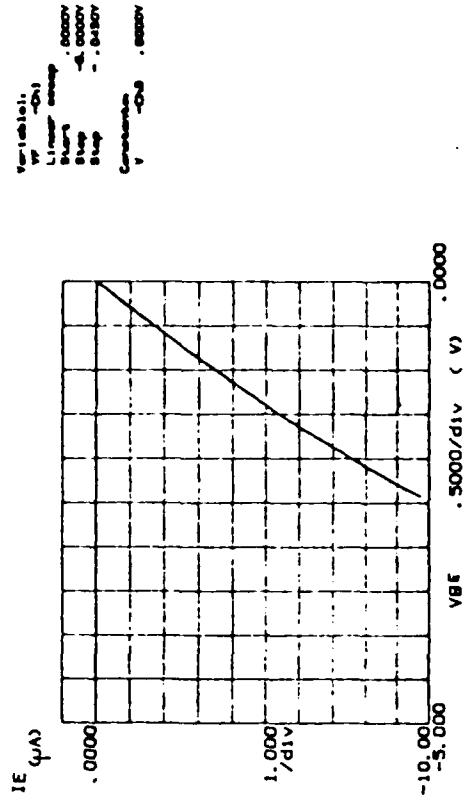
***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****



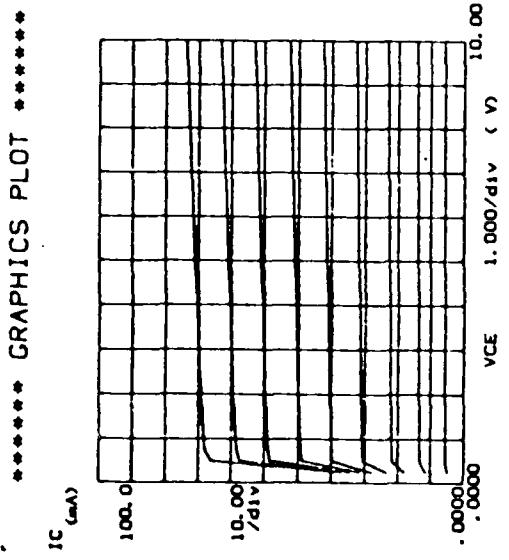
Variables:
 V_{CE} - Chg
 I_{CE} - Chg
 H_F - Chg
 V_{BE} - Chg
 I_E - Chg
 V_{CE} - Show
 I_{CE} - Show
 H_F - Show
 V_{BE} - Show
 I_E - Show
 V_{CE} - Comprom
 I_{CE} - Comprom
 H_F - Comprom
 V_{BE} - Comprom
 I_E - Comprom

***** GRAPHICS PLOT *****



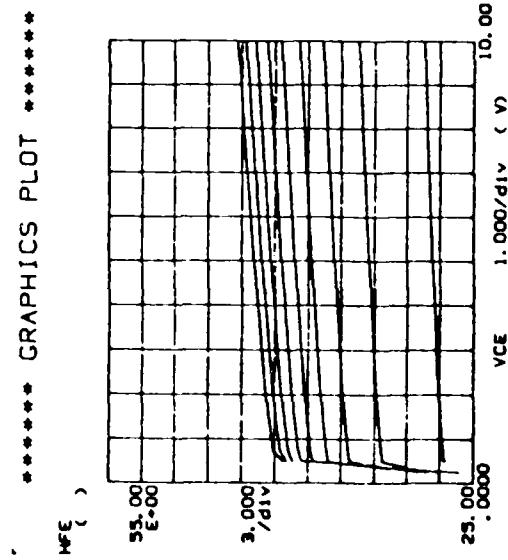
Variables:
 V_{CE} - Chg
 I_{CE} - Chg
 H_F - Chg
 V_{BE} - Chg
 I_E - Chg
 V_{CE} - Show
 I_{CE} - Show
 H_F - Show
 V_{BE} - Show
 I_E - Show
 V_{CE} - Comprom
 I_{CE} - Comprom
 H_F - Comprom
 V_{BE} - Comprom
 I_E - Comprom

Figs. B.1.e



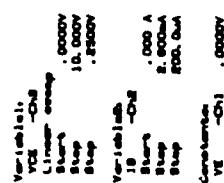
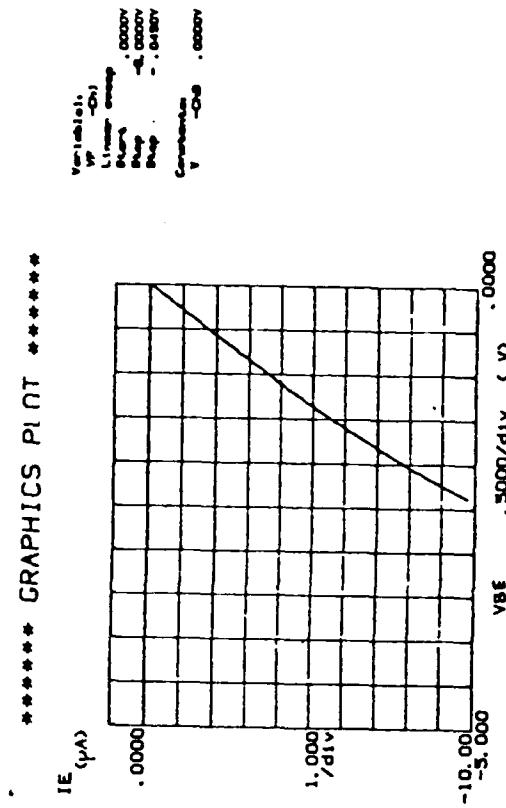
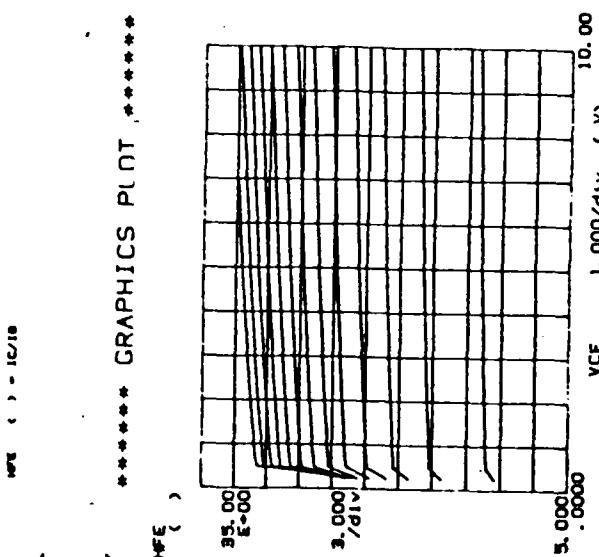
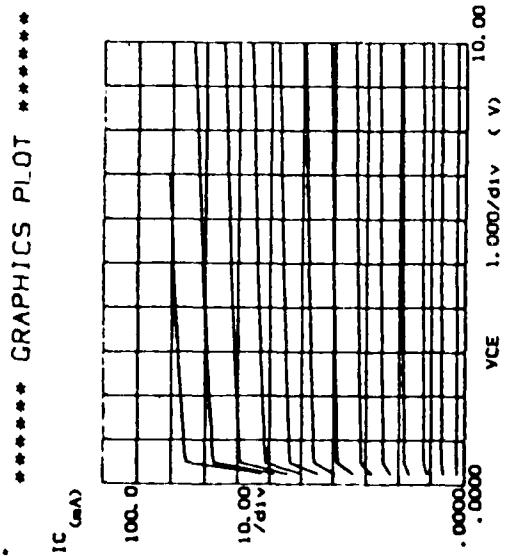
MPW (1 → 10/10)

- 73 -



MPW (1 → 10/10)

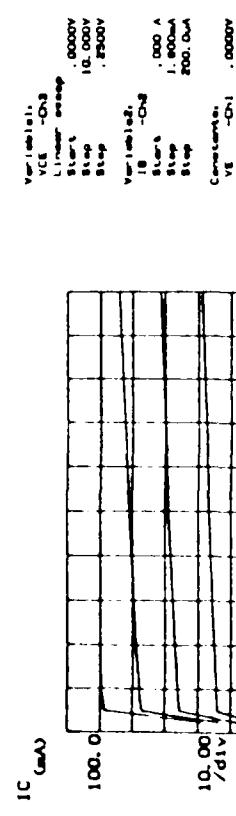
Figs. B.1.f



卷之三

Figs. B.2.a

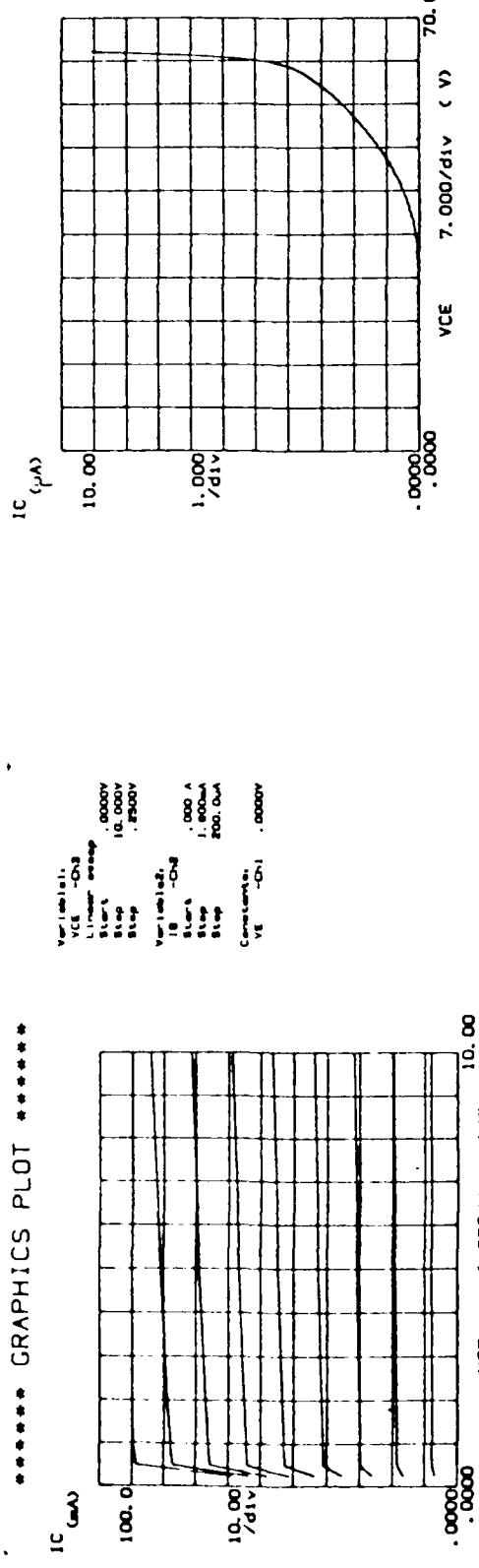
***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****

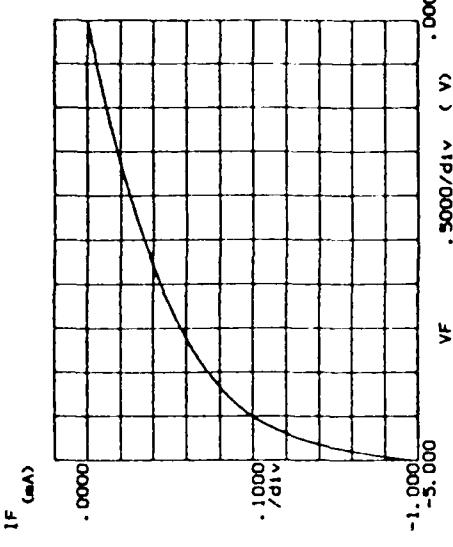


***** GRAPHICS PLOT *****



NOTE: 1 → 1C/10

***** GRAPHICS PLOT *****



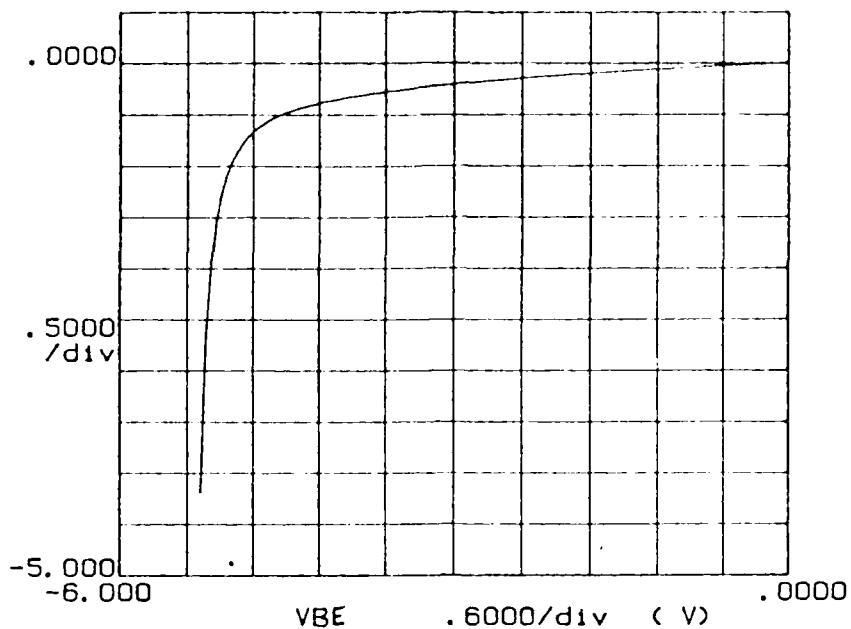
NOTE: 1 → 1C/10

Variable list:
 VCE - Ch1
 Linear sweep
 Start 0.000V
 Stop 10.000V
 Step 0.1000V
 V_B - Ch1
 Start 0.000A
 Stop 1.000A
 Step 0.0001A
 Current limit 200.0mA
 VF - Ch1 .0000V

Variable list:
 VCE - Ch1
 Linear sweep
 Start 0.000V
 Stop 10.000V
 Step 0.1000V
 V_B - Ch1
 Start 0.000A
 Stop 1.000A
 Step 0.0001A
 Current limit 200.0mA
 VF - Ch1 .0000V

***** GRAPHICS PLOT *****

IE
(mA)

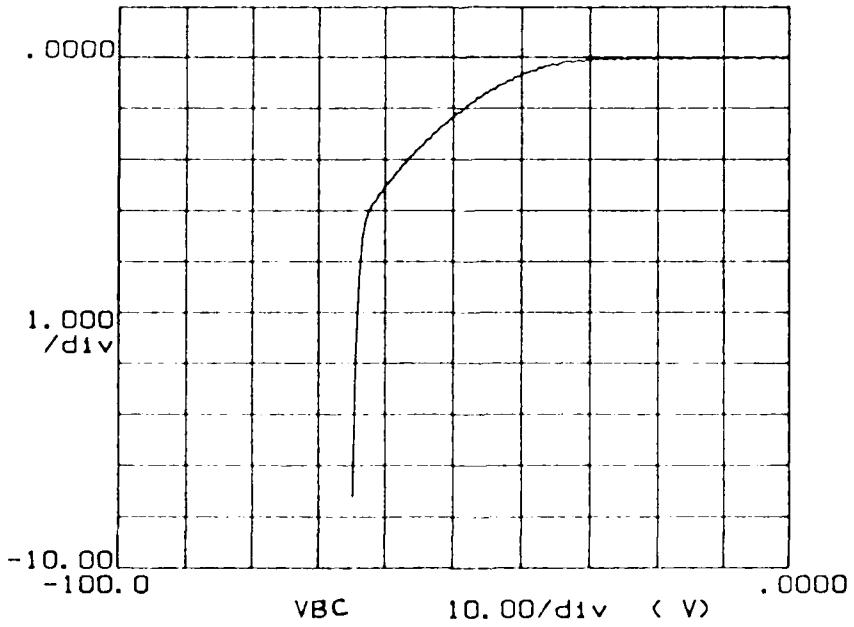


Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop -.06.0000V
Step -.0480V

Constants:
V -Ch3 .0000V

***** GRAPHICS PLOT *****

IC
(μ A)

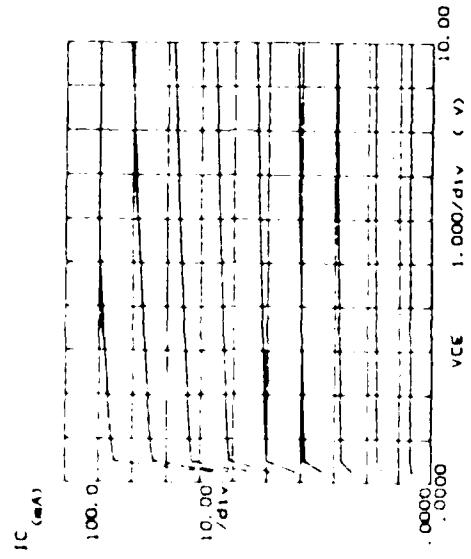


Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop -100.00V
Step -.5000V

Constants:
V -Ch3 .0000V

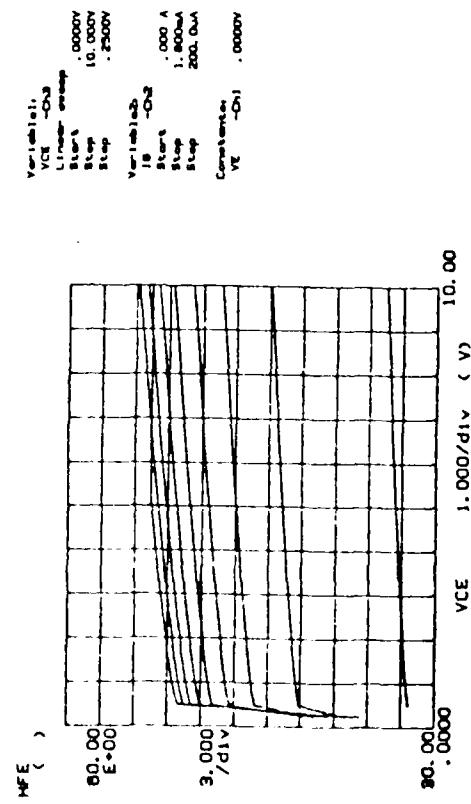
Figs. B.2.b

***** GRAPHICS PLOT *****



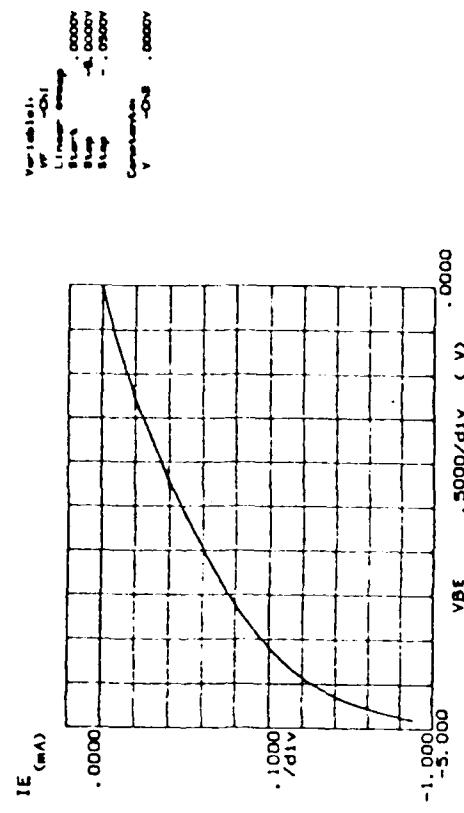
$\text{curve } (1) \rightarrow I_C/10$

***** GRAPHICS PLOT *****



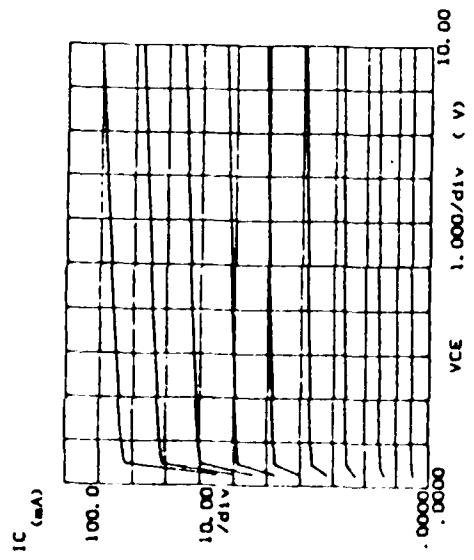
$\text{curve } (1) \rightarrow I_C/10$

***** GRAPHICS PLOT *****

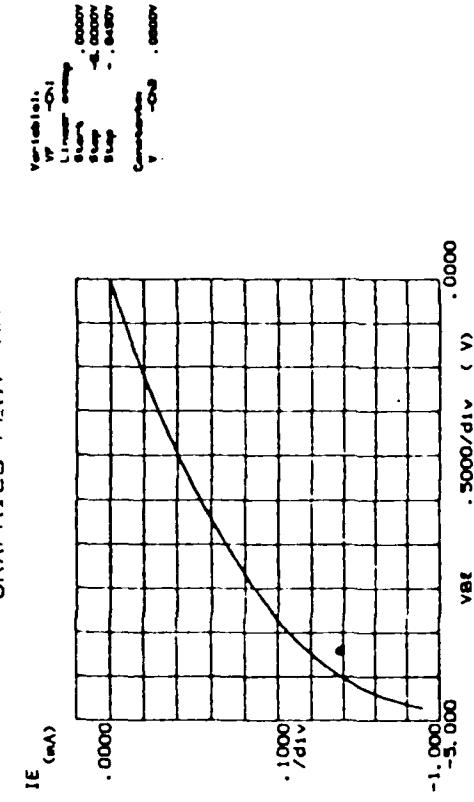


Figs. B.2.c

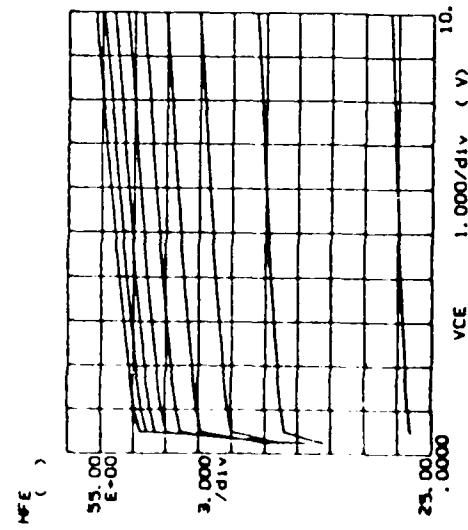
***** GRAPHICS PLOT *****



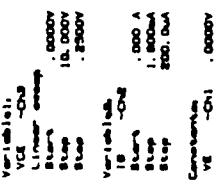
***** GRAPHICS PLOT *****



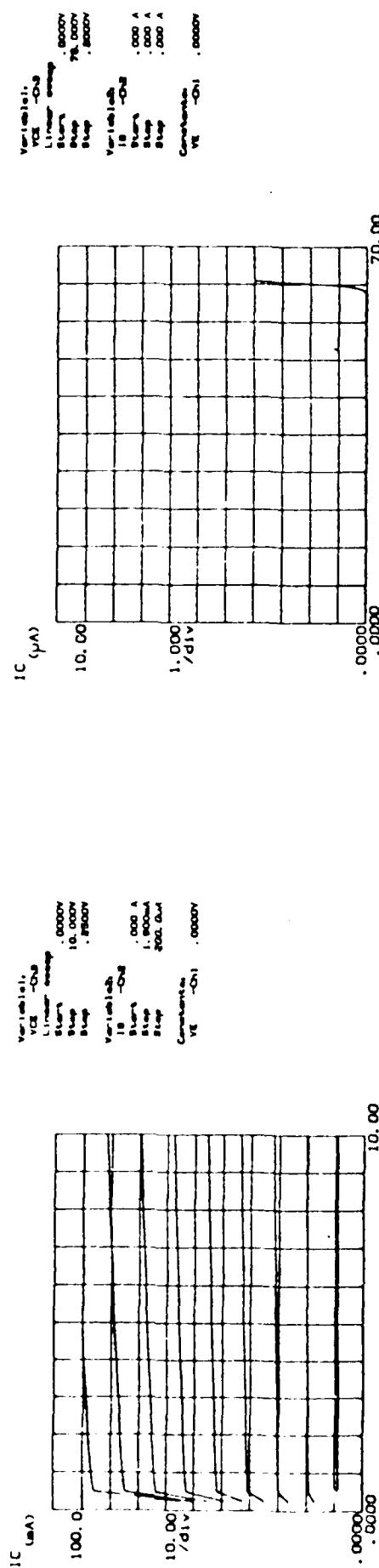
***** GRAPHICS PLOT *****



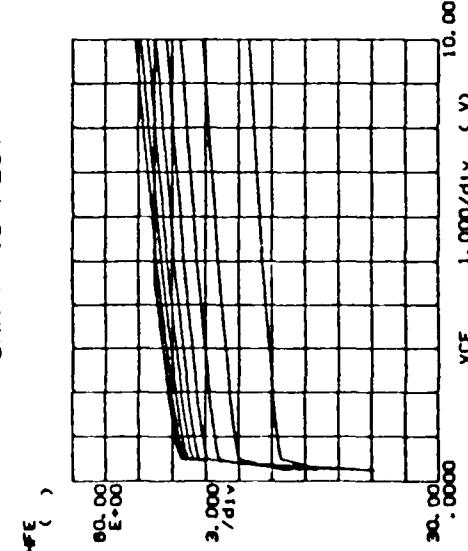
***** GRAPHICS PLOT *****



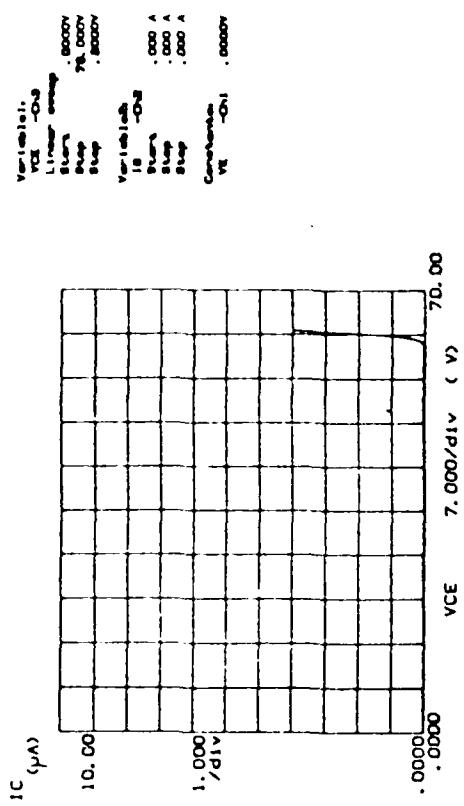
***** GRAPHICS PLOT *****



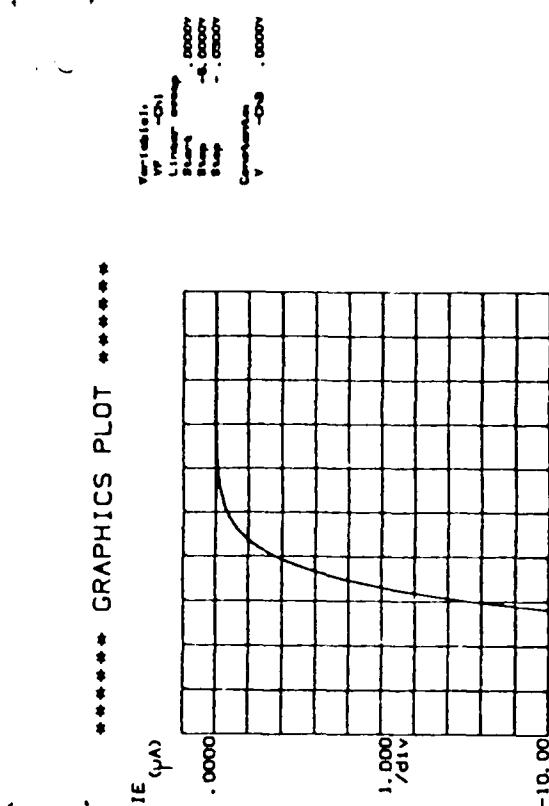
***** GRAPHICS PLOT *****
***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****

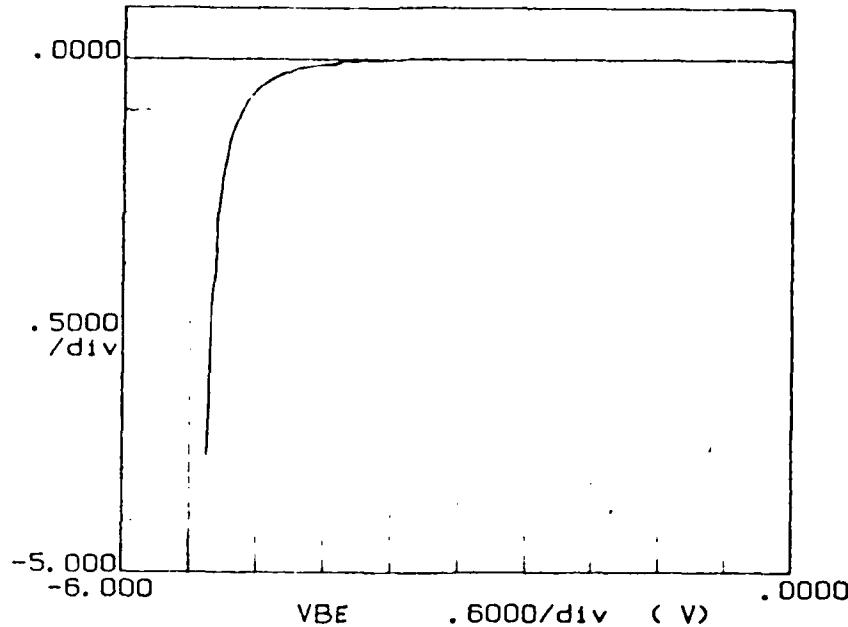


***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****

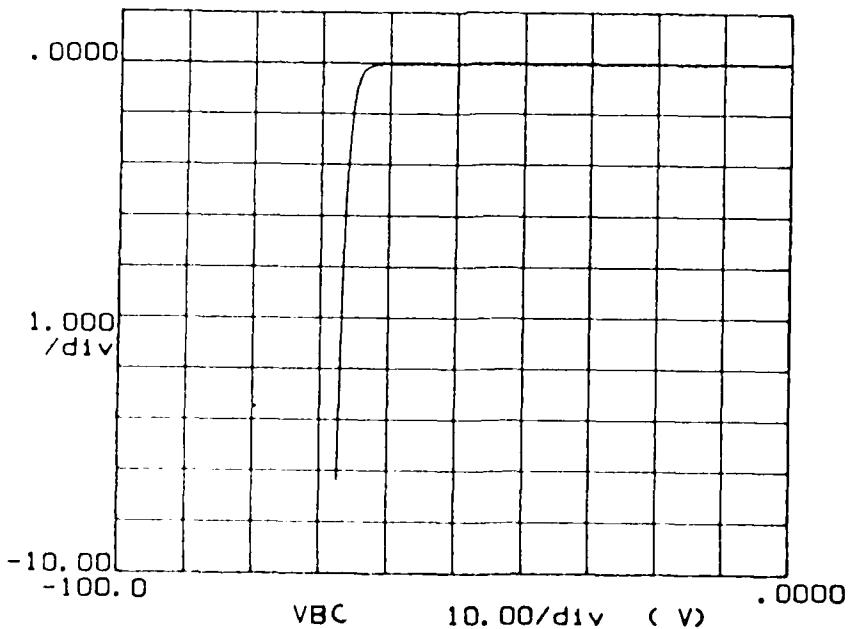
IE
(mA)



Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop -6.0000V
Step -.0500V

Constants:
V -Ch3 .0000V

IC
(μ A.)

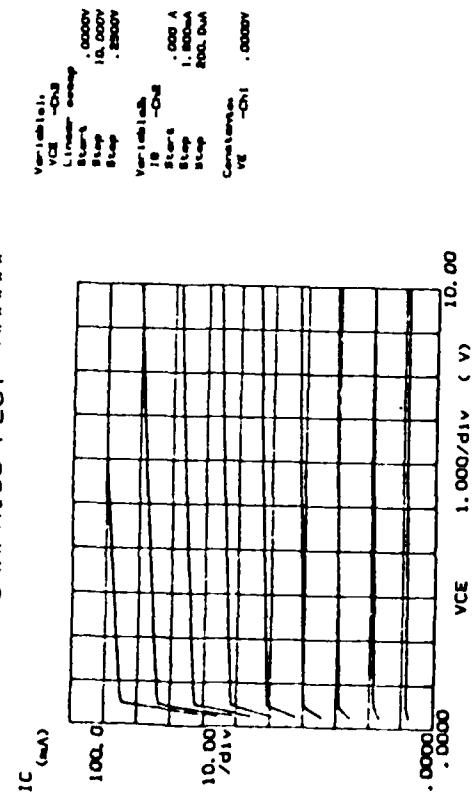


Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop -100.00V
Step -.5000V

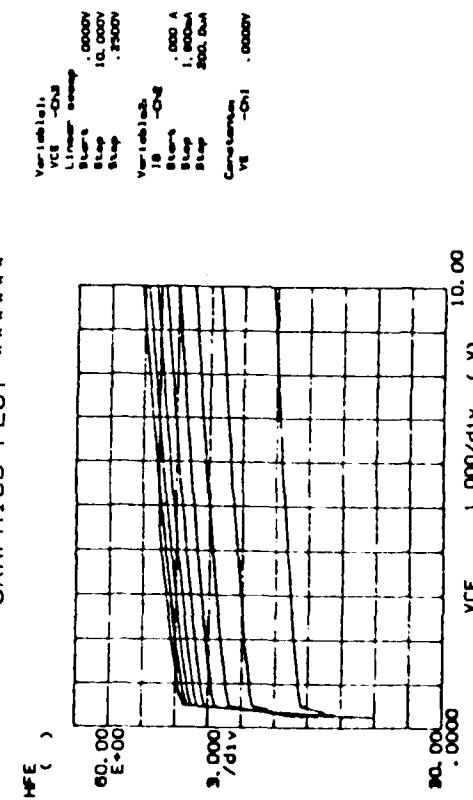
Constants:
V -Ch3 .0000V

Figs. B.3.d

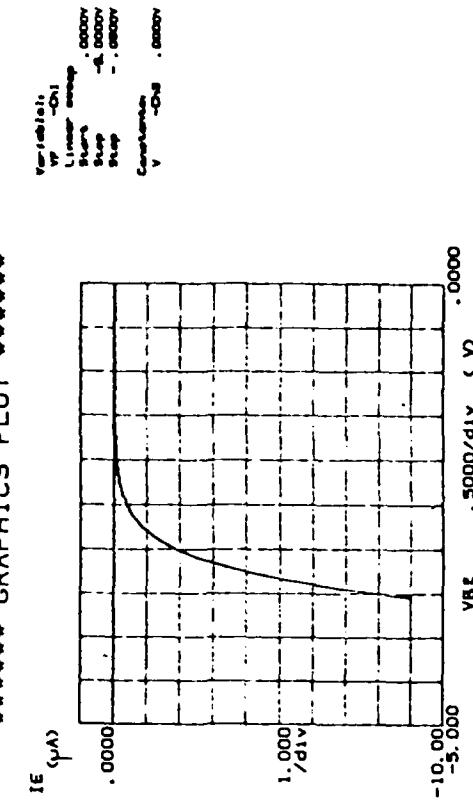
***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****

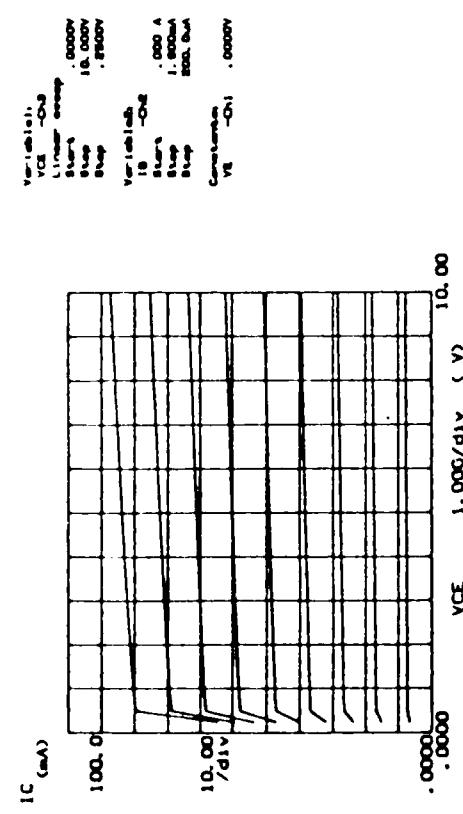


***** GRAPHICS PLOT *****

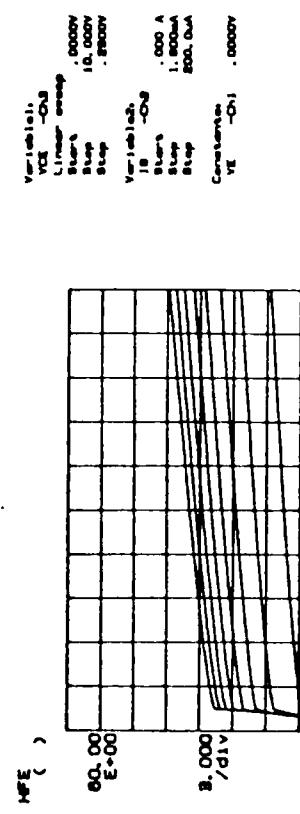


Figs. B.4.a

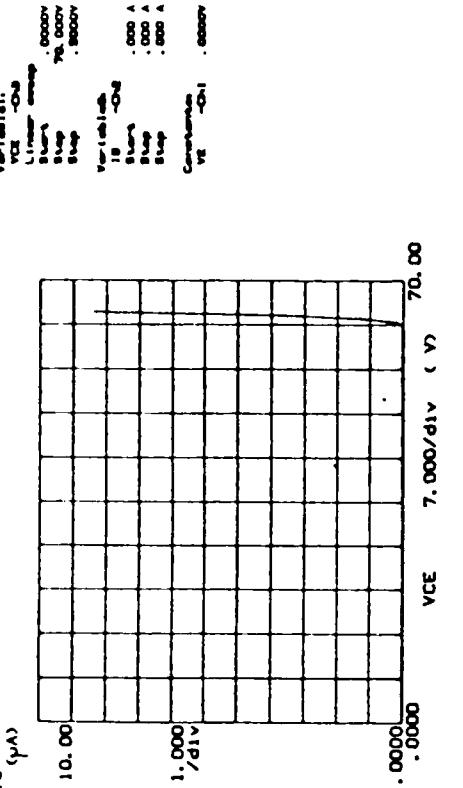
***** GRAPHICS PLOT *****



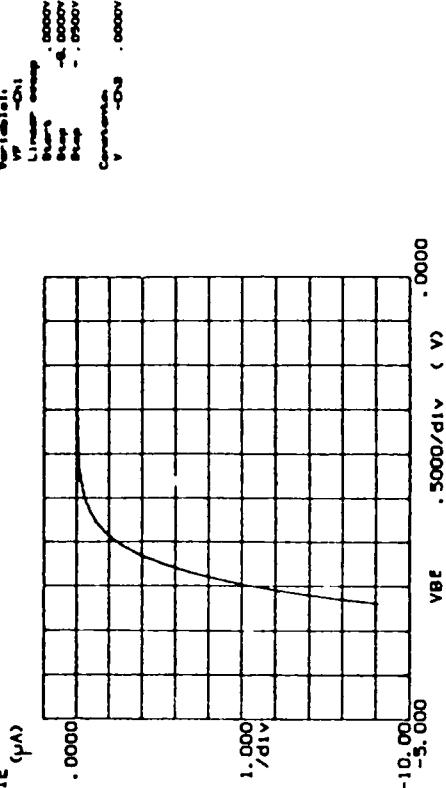
***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****

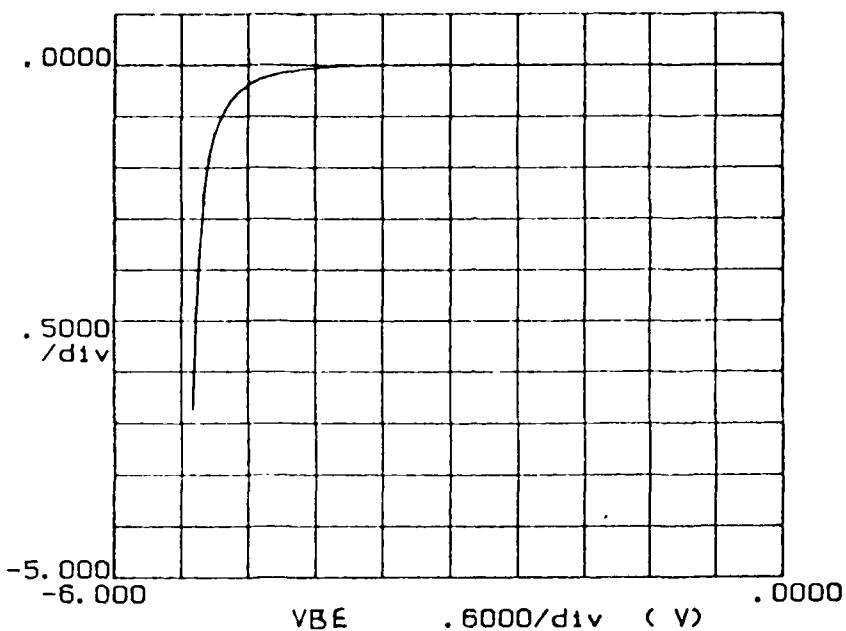


***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****

IE
(mA)

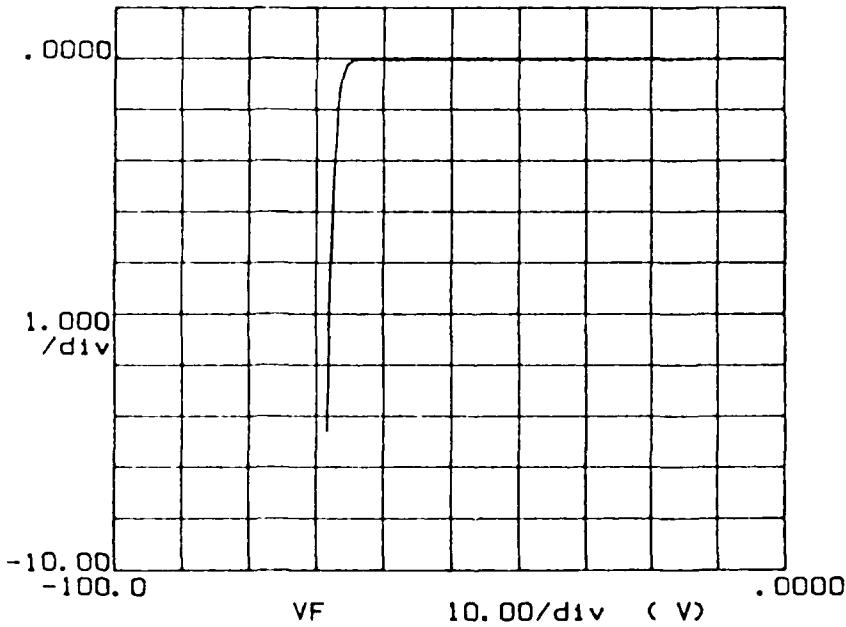


Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop -6.0000V
Step -.0500V

Constants:
V -Ch3 .0000V

***** GRAPHICS PLOT *****

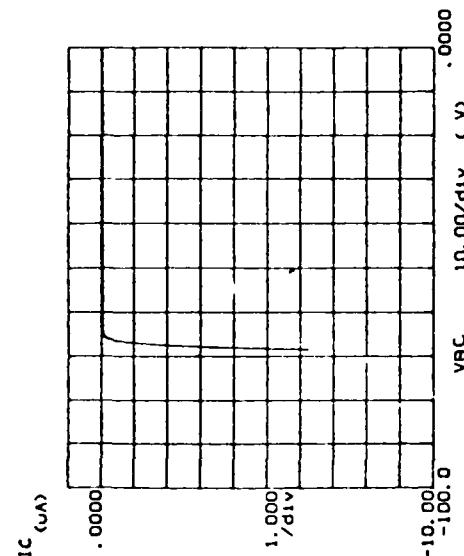
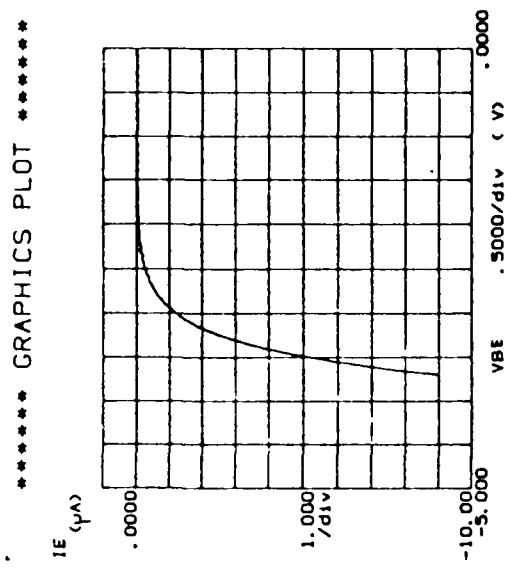
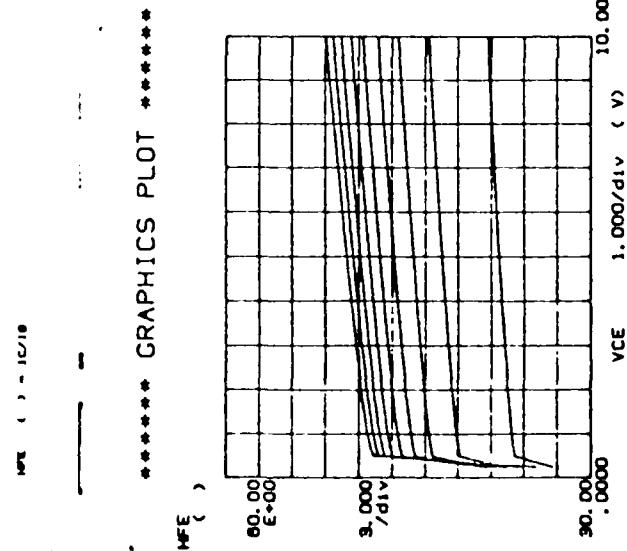
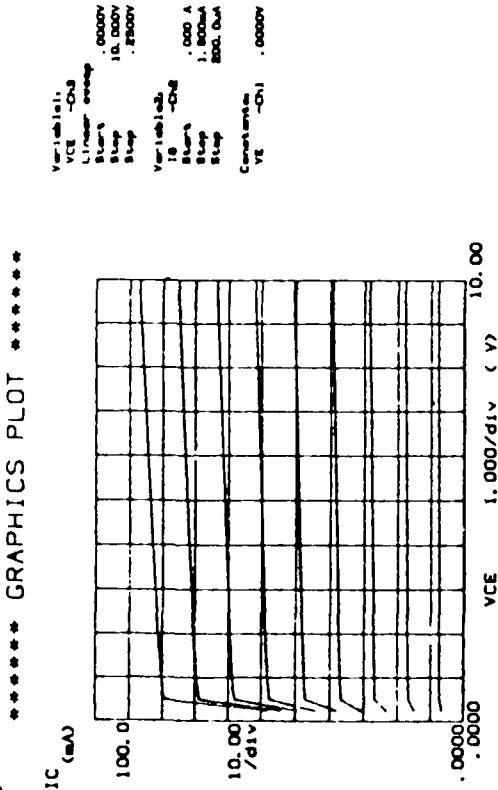
IC
(uA)



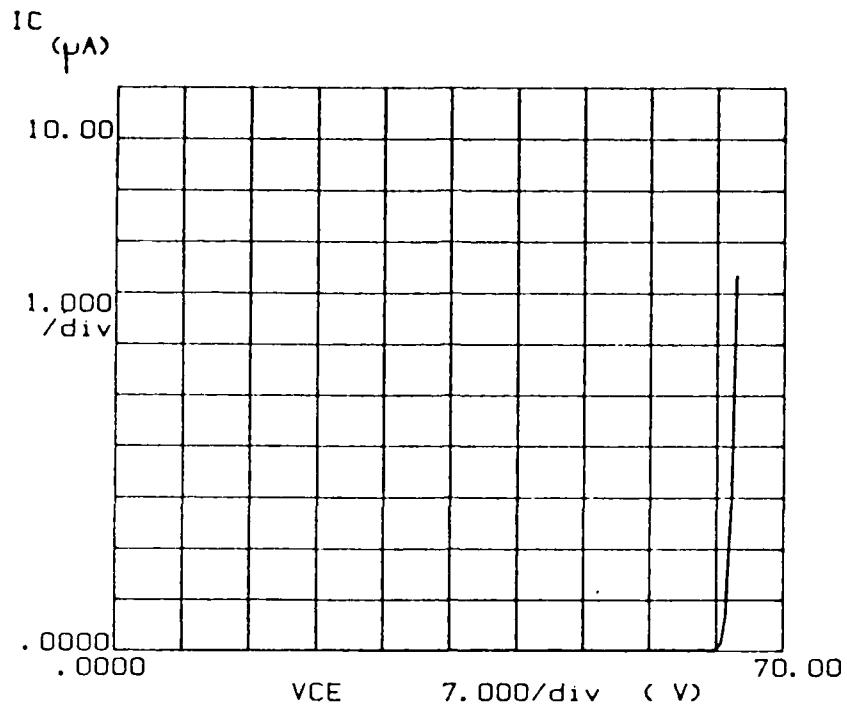
Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop -100.00V
Step -.5000V

Constants:
V -Ch3 .0000V

Figs. B.4.e



***** GRAPHICS PLOT *****



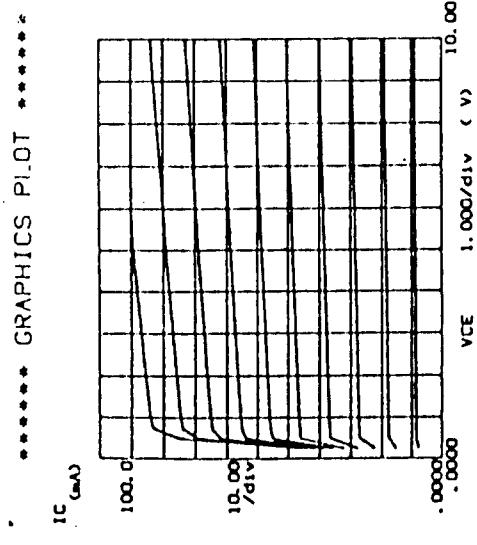
Variables:
VCE -Ch3
Linear sweep
Start .0000V
Stop 70.000V
Step .5000V

Variable2:
IB -Ch2
Start .000 A
Stop .000 A
Step .000 A

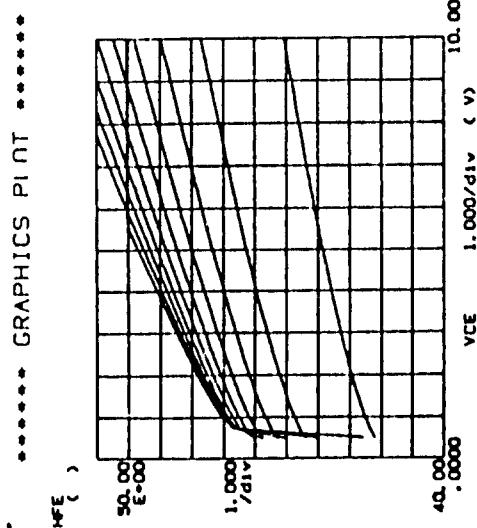
Constants:
VE -Ch1 .0000V

HFE () = IC/IB

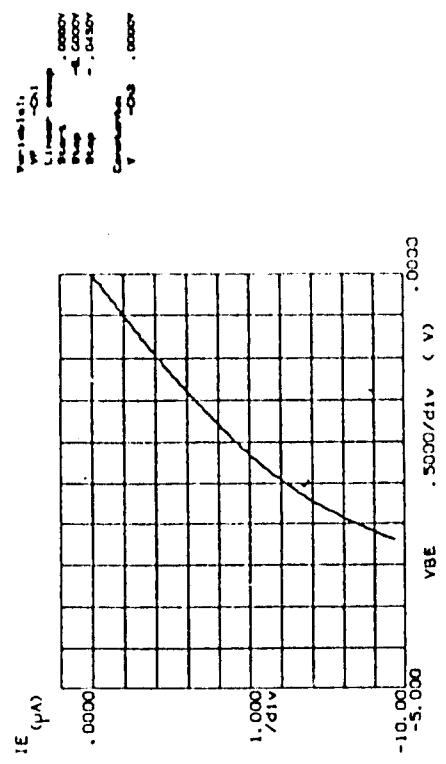
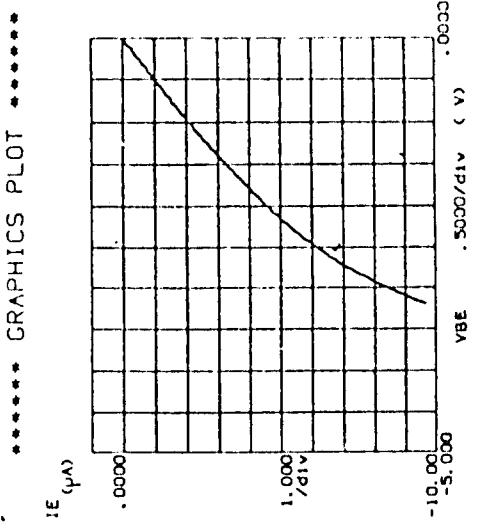
Figs. C.1.a



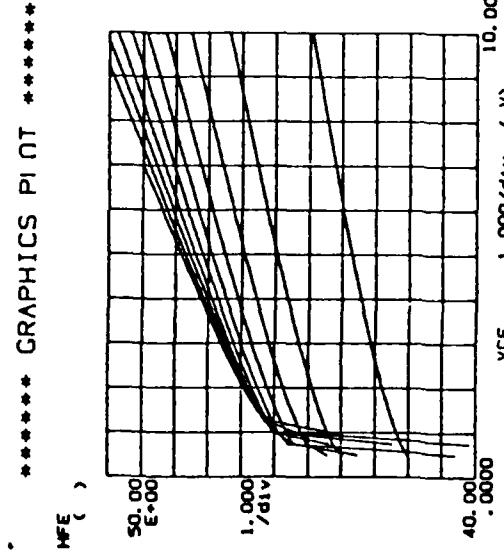
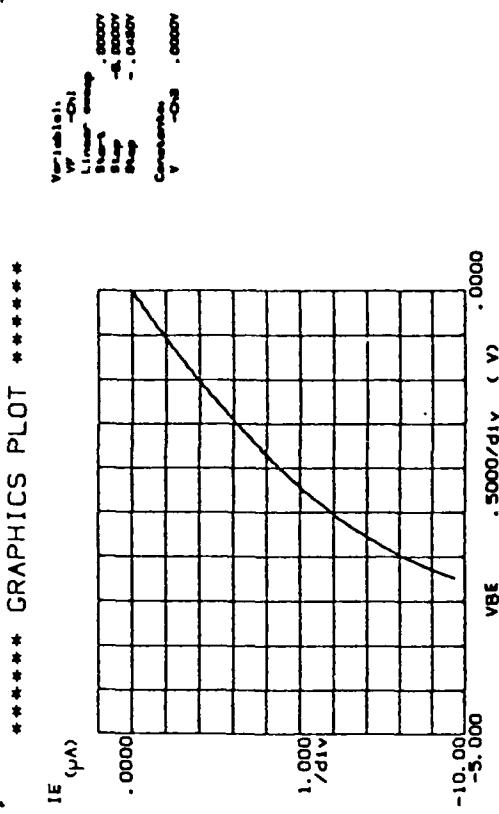
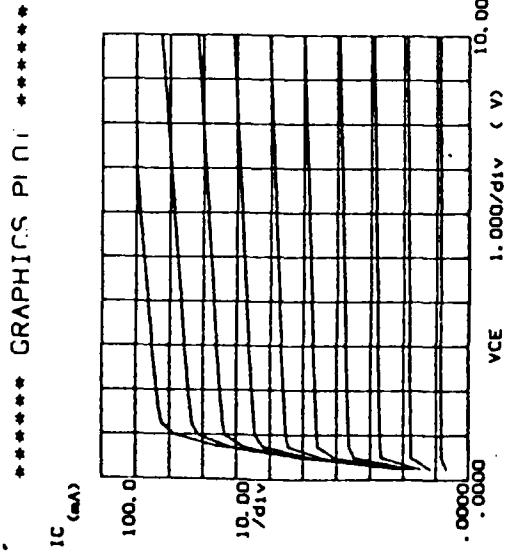
IB = -1E-08



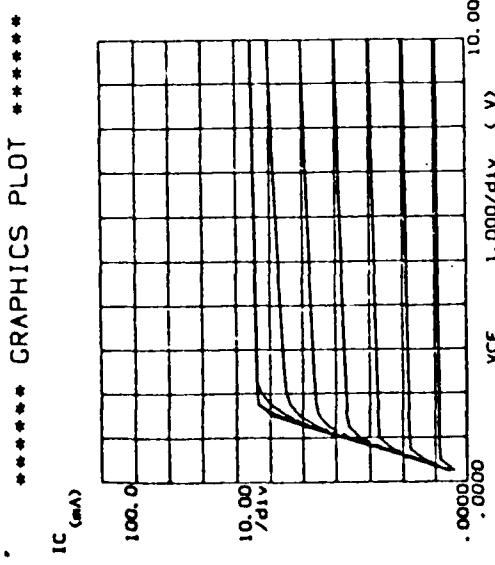
IB = -1E-08



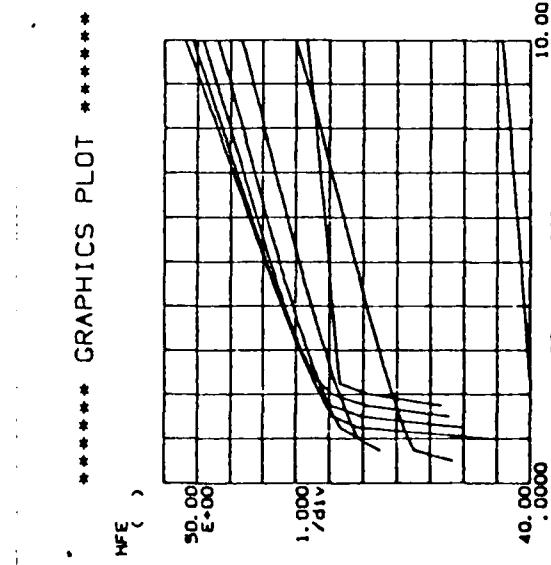
Figs. C.1.c



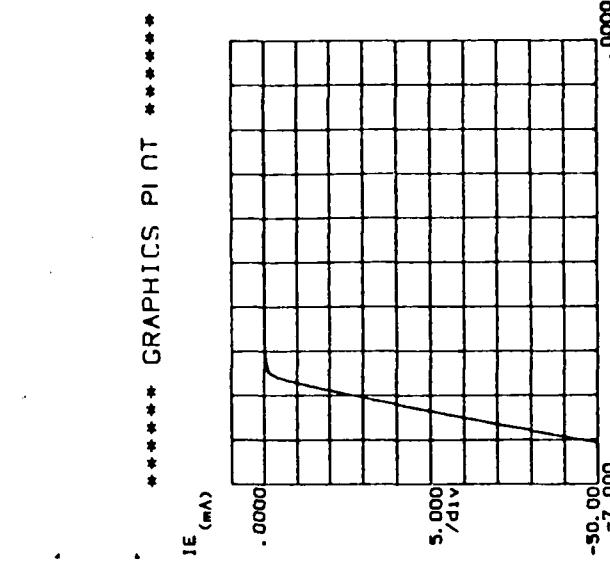
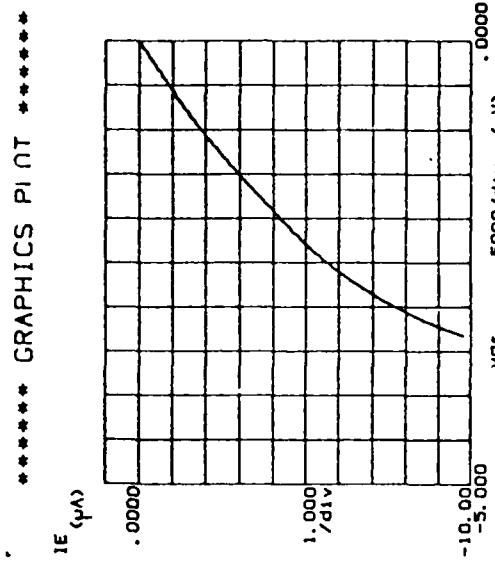
Figs. C.1.d



HFE ()



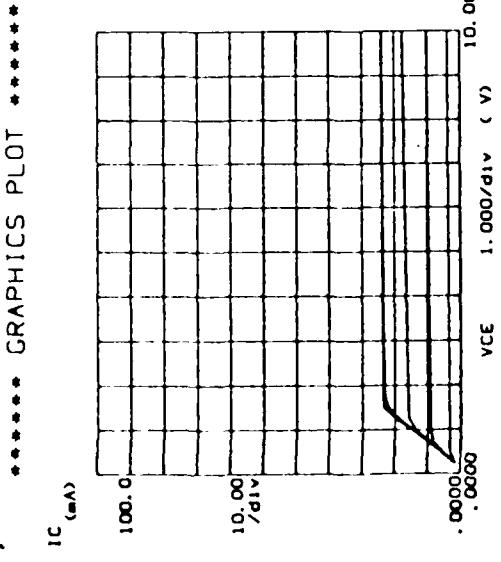
HFE ()



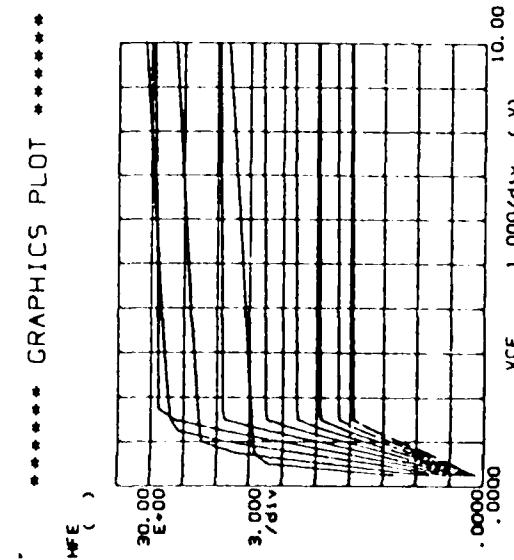
***** GRAPHICS PLOT *****

***** GRAPHICS PLOT *****

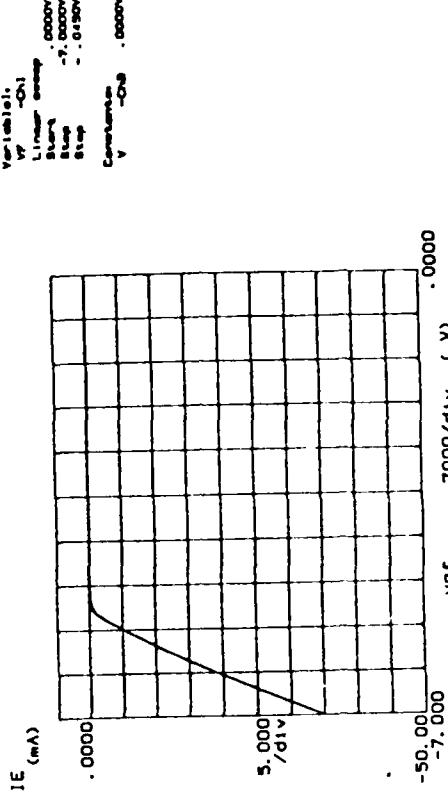
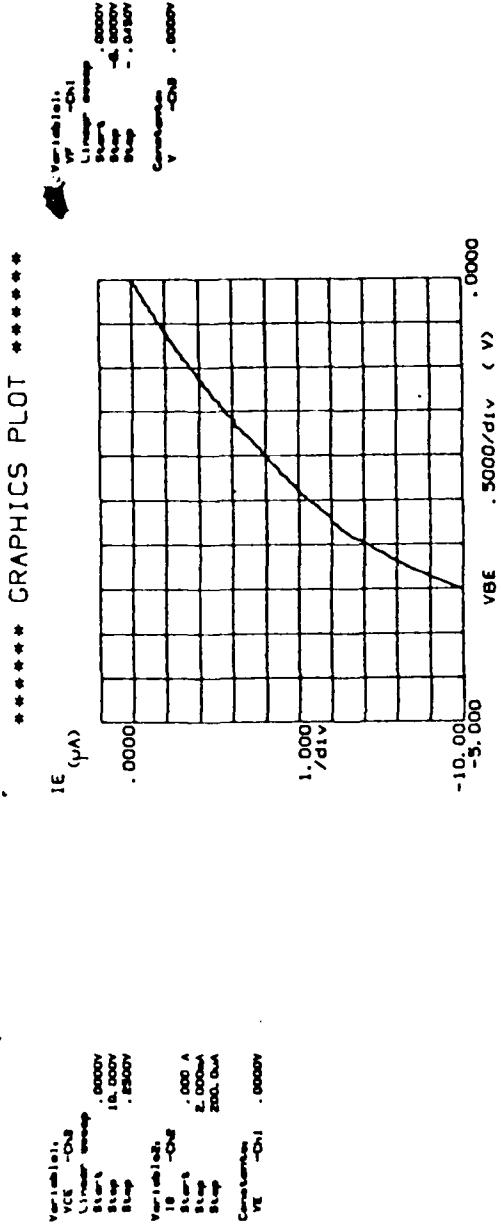
Figs. C.1.e



*** - 100 ***

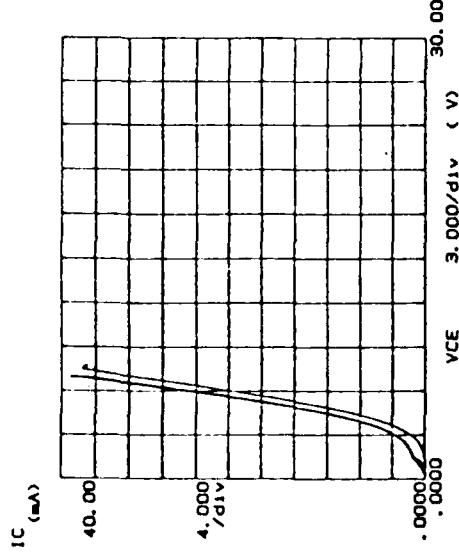


- 100 -

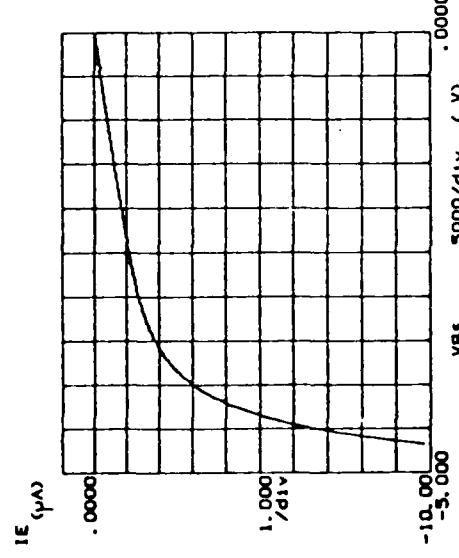


Figs. C.1.f

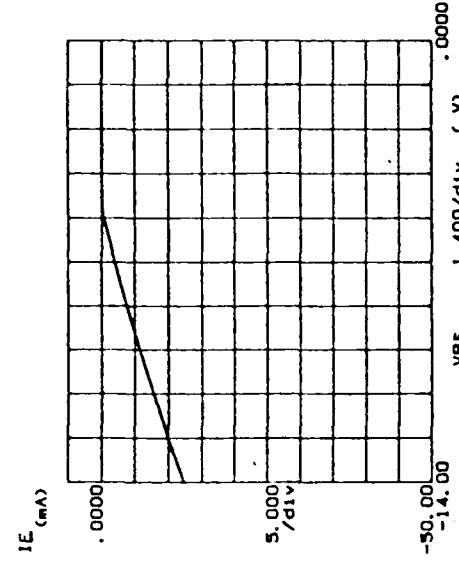
***** GRAPHICS PLOT *****



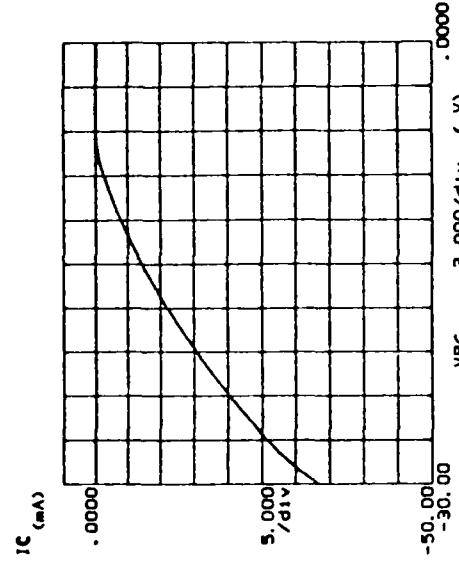
***** GRAPHICS PLOT *****



***** GRAPHICS PLOT *****



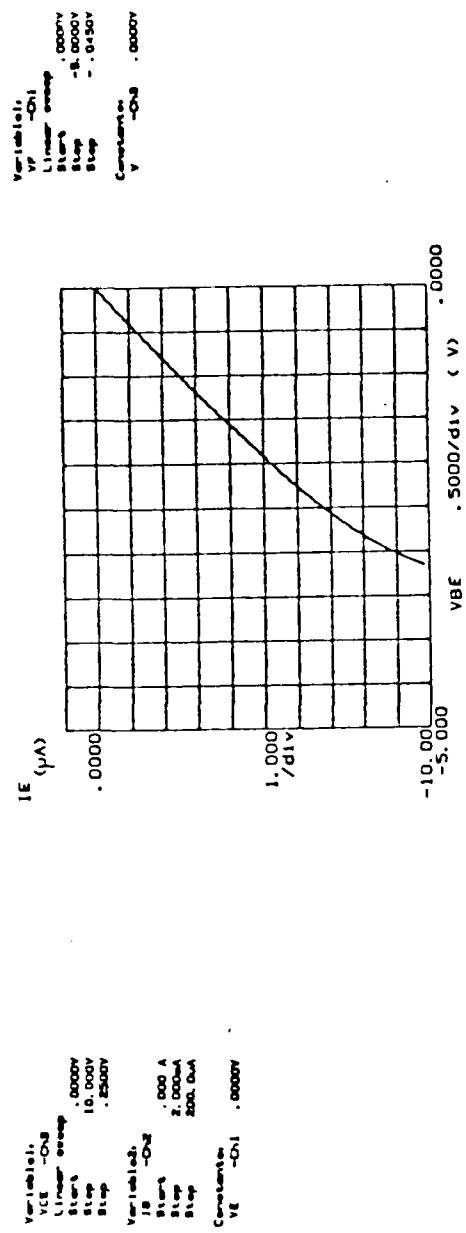
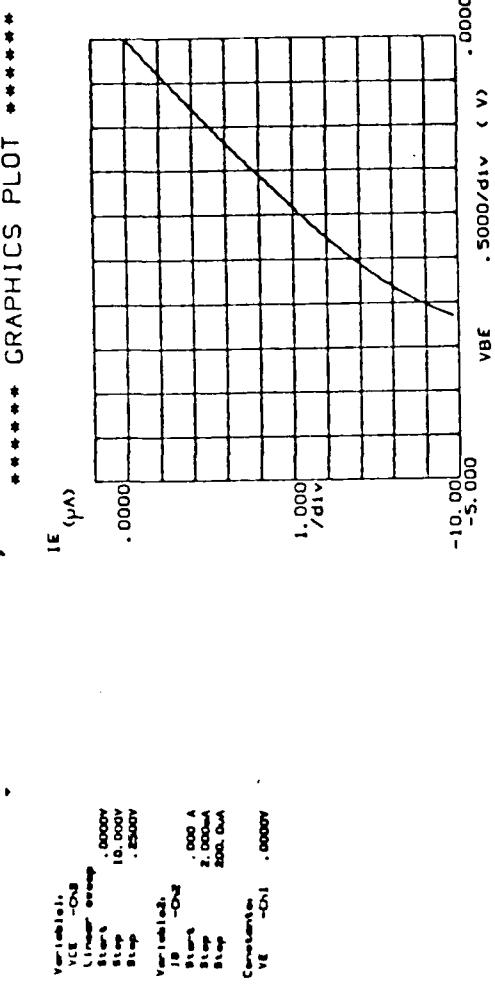
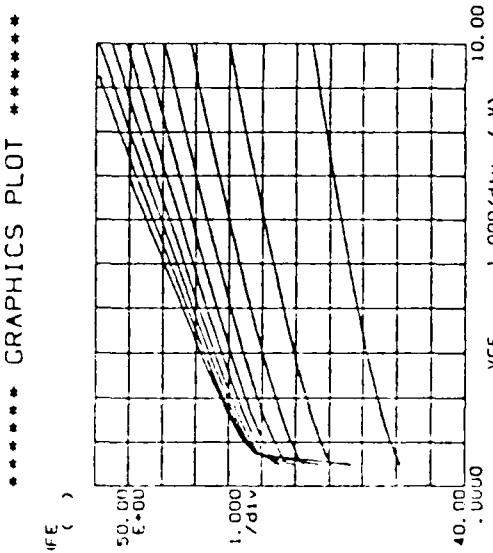
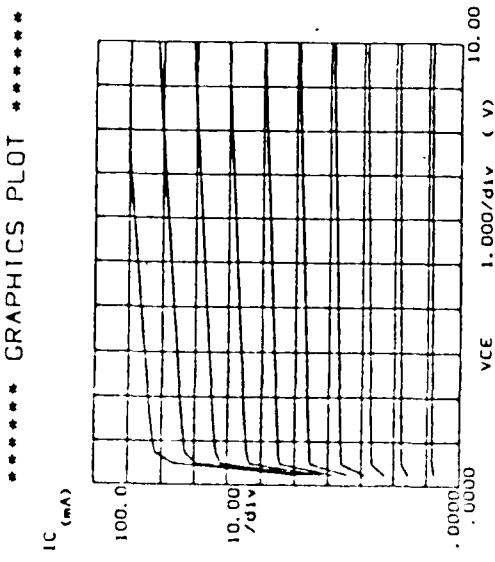
***** GRAPHICS PLOT *****



Variables:
 V_{CE} -Ch1
 Linear sweep
 Start 0.000V
 Stop 10.000V
 Step 0.00001V
 Incr 1.000A
 Scale 1.000A
 Units mA
 Conv/Div -Ch1 .0000V

Variables:
 V_{BE} -Ch1
 Linear sweep
 Start 0.000V
 Stop 10.000V
 Step 0.00001V
 Incr 1.000A
 Scale 1.000A
 Units mA
 Conv/Div -Ch1 .0000V

Figs. C.2.a



Figs. C.2.b

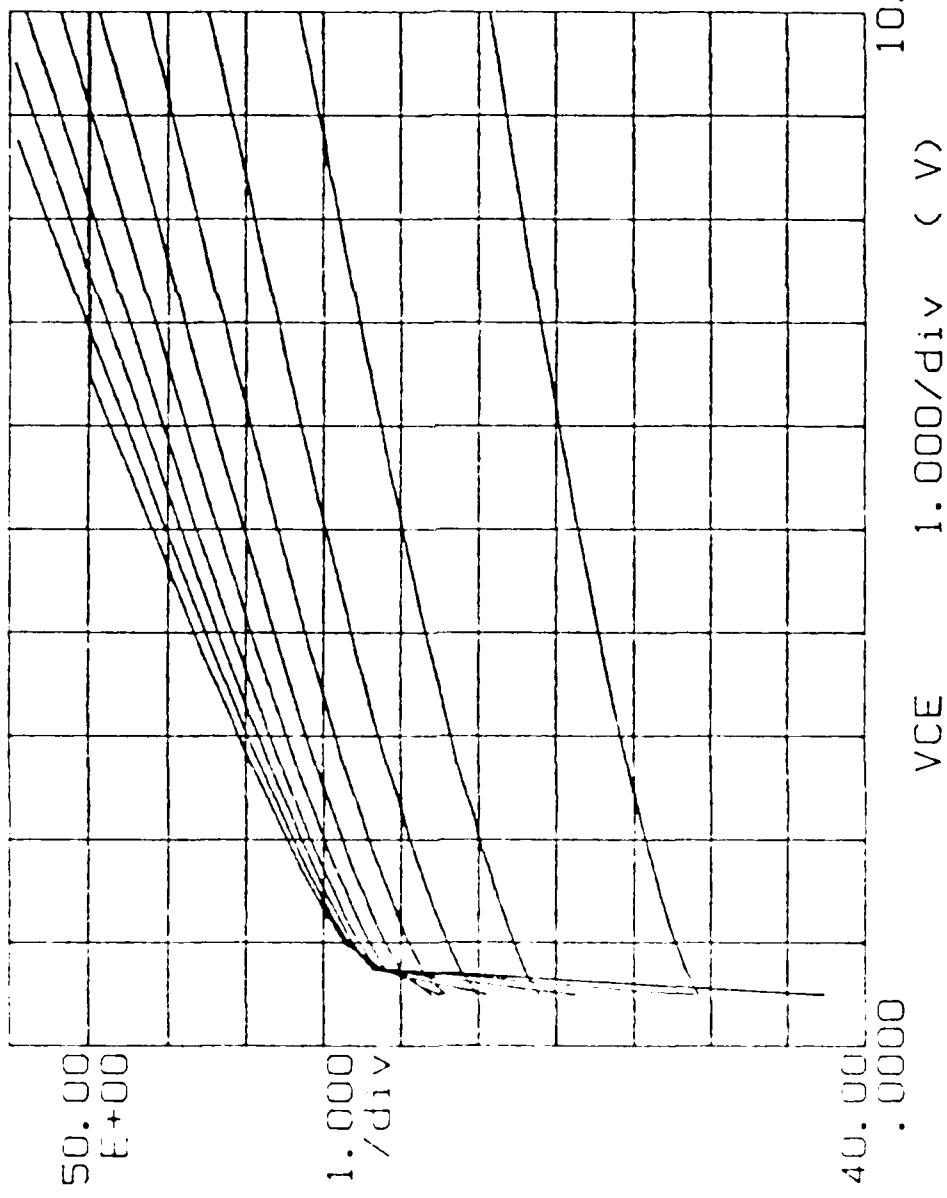
***** GRAPHICS PLOT *****

HFE
()

Variables:
VCE -Ch3
Linear sweep
Start : 0000V
Stop 10.000V
Step .2500V

Variables:
IB -Ch2
Start .000 A
Stop 2.000mA
Step 200.0mA

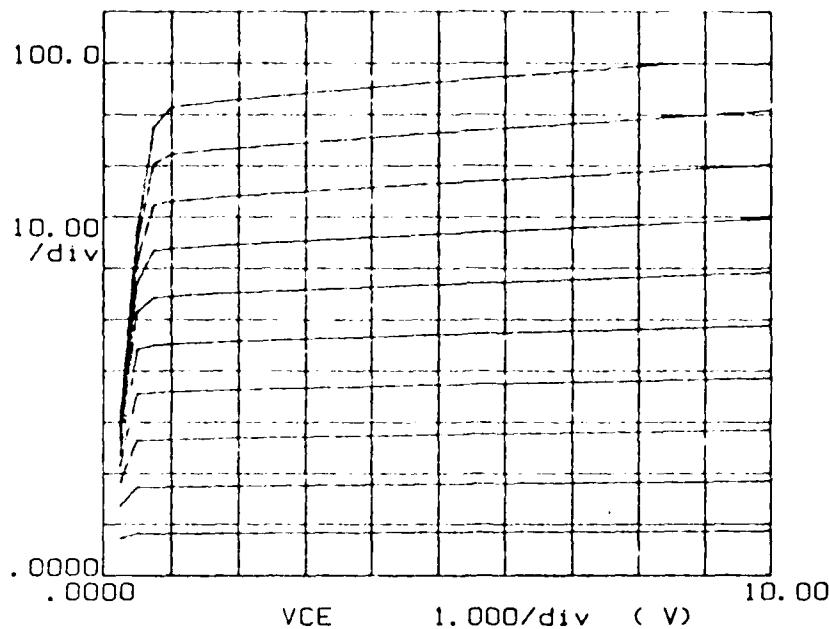
Constant:
VE -Ch1 .0000V



Figs. C.2.c

***** GRAPHICS PLOT *****

IC
(mA)



Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

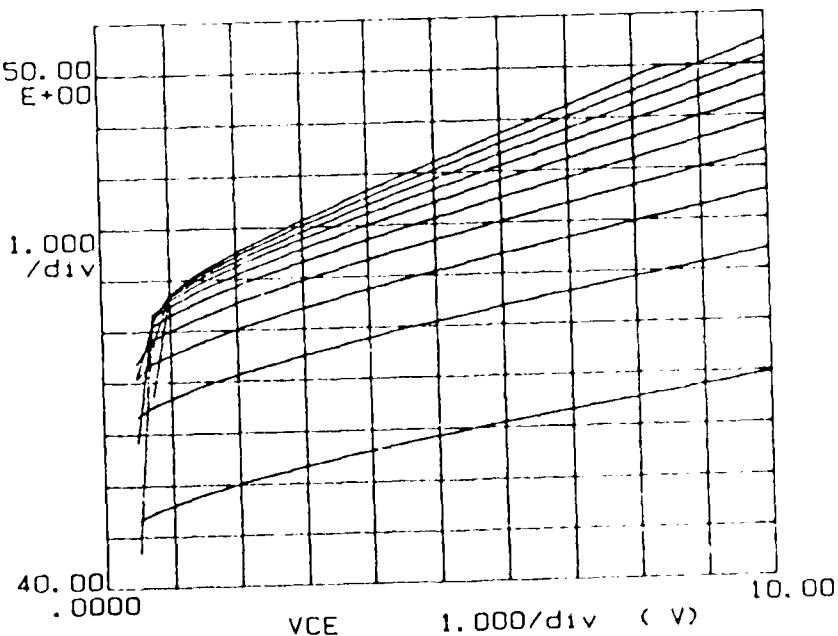
Variable2:
IB -Ch2
Start .000 A
Stop 2.000mA
Step 200.0uA

Constant:
VE -Ch1 .0000V

HFE () = IC/IB

***** GRAPHICS PLOT *****

HFE
()



Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

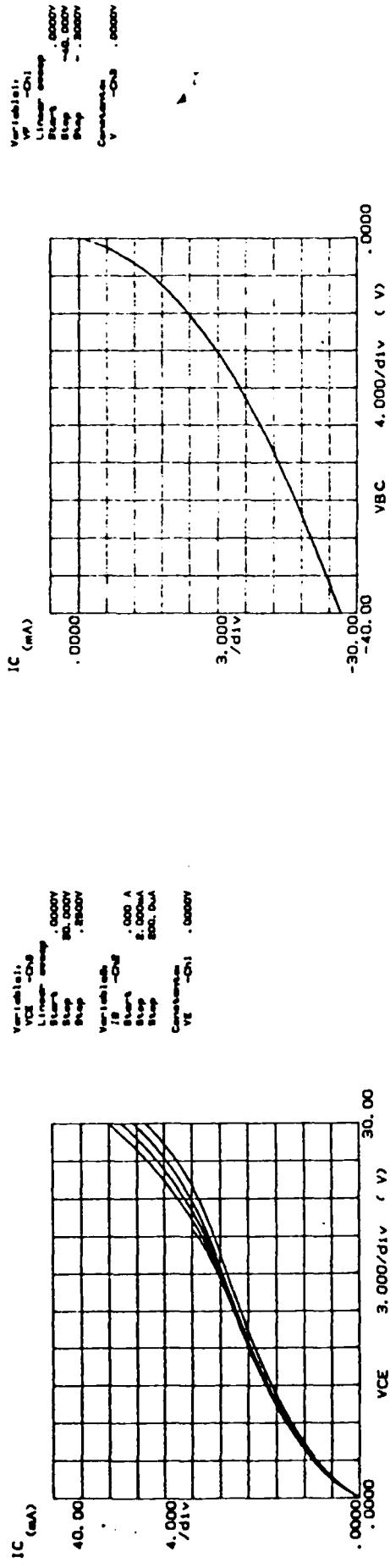
Variable2:
IB -Ch2
Start .000 A
Stop 2.000mA
Step 200.0uA

Constant:
VE -Ch1 .0000V

HFE () = IC/IB

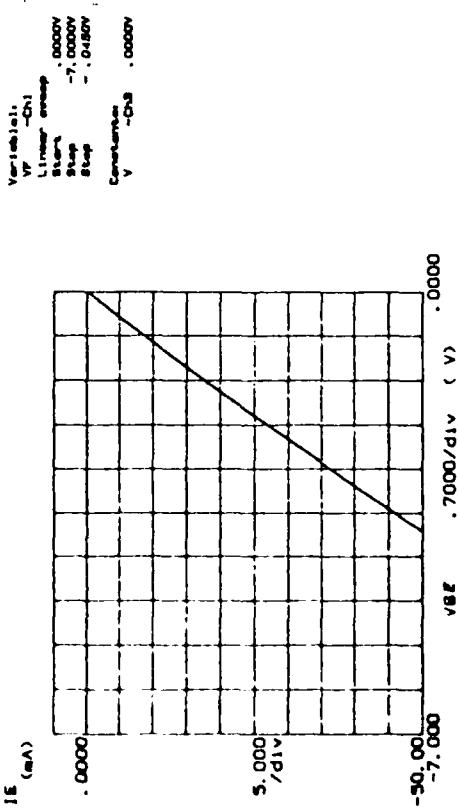
Figs. C.2.d

***** GRAPHICS PLOT *****

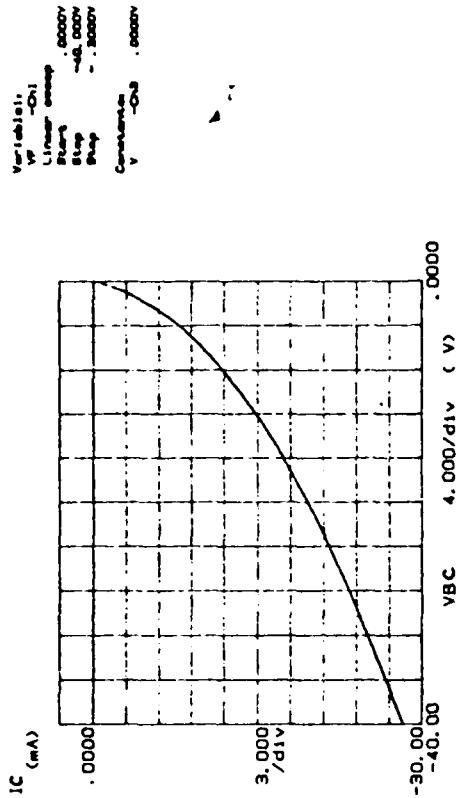


IC = IC/10

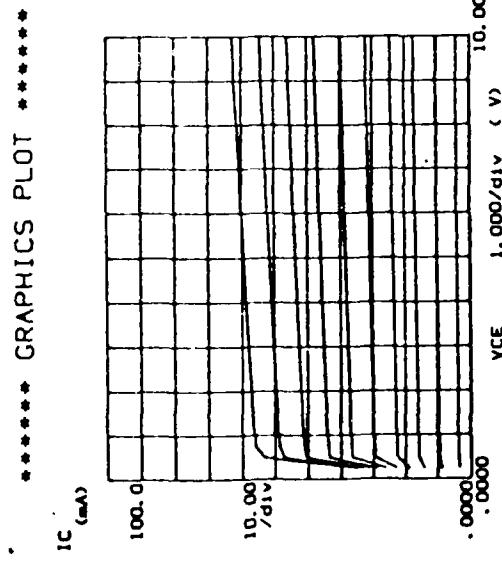
***** GRAPHICS PLOT *****



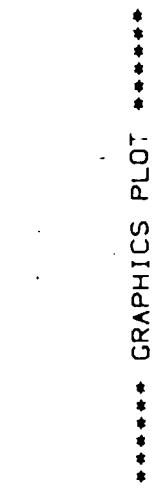
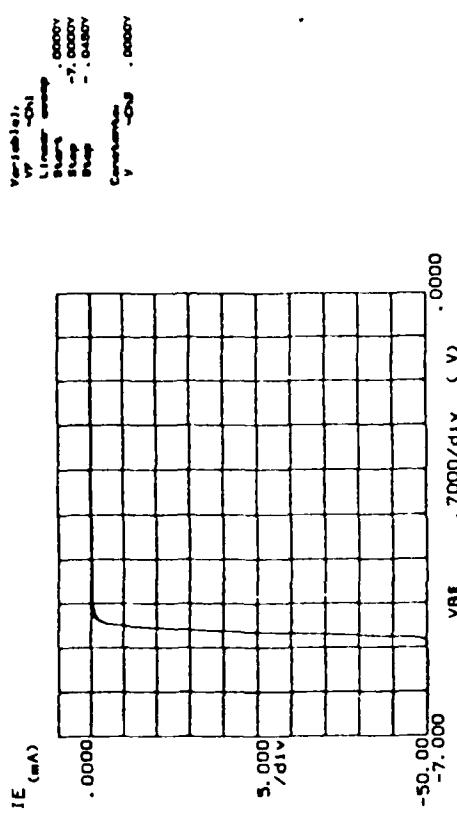
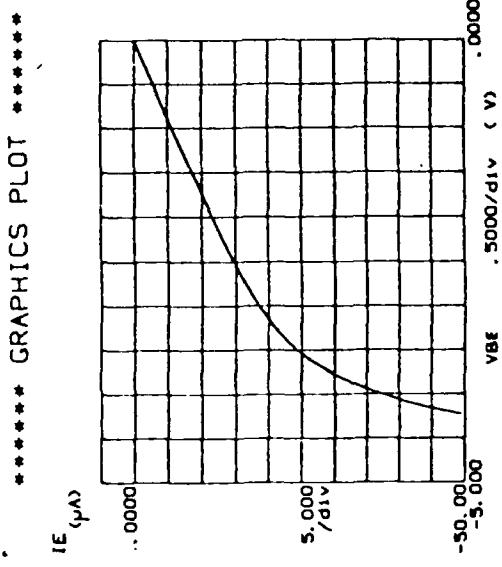
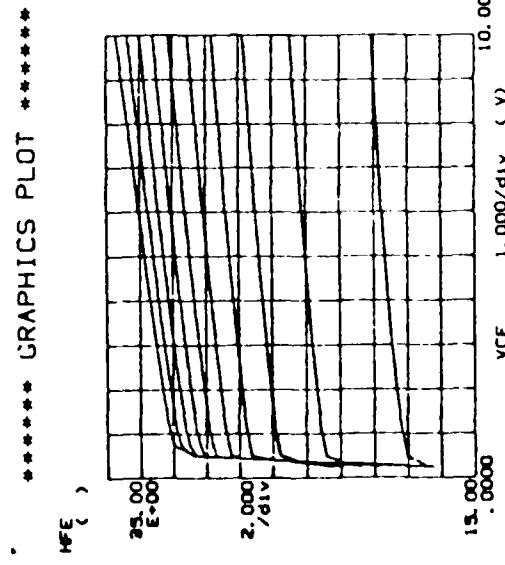
***** GRAPHICS PLOT *****



Figs. C.3.a

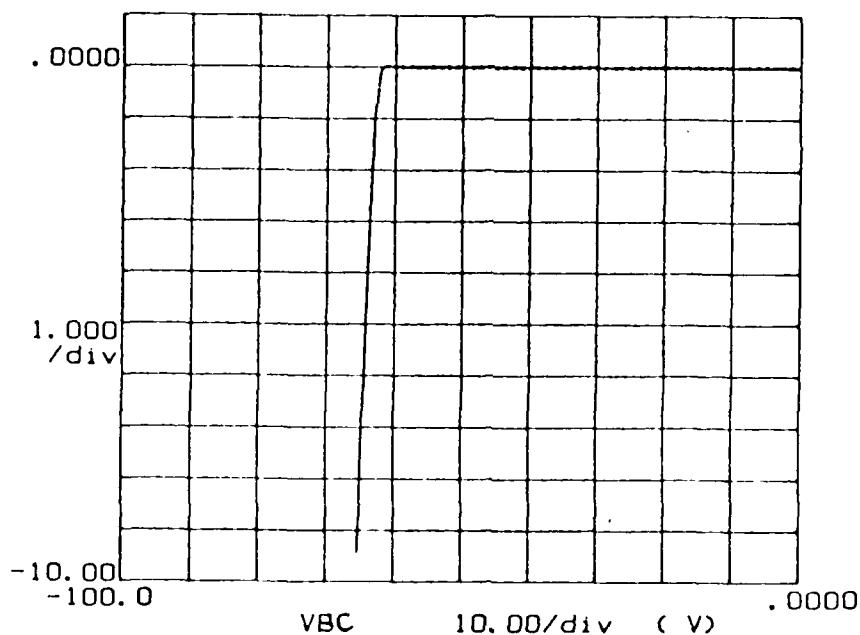


WIRE () - 1E/10



***** GRAPHICS PLOT *****

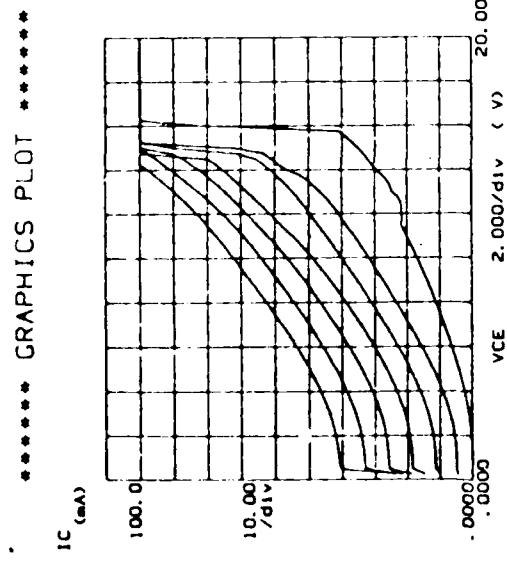
IC
(μ A)



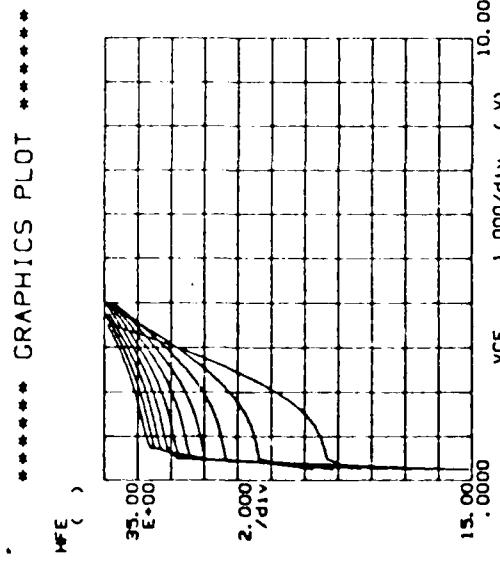
Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop -100.00V
Step -.2000V

Constants:
V -Ch3 .0000V

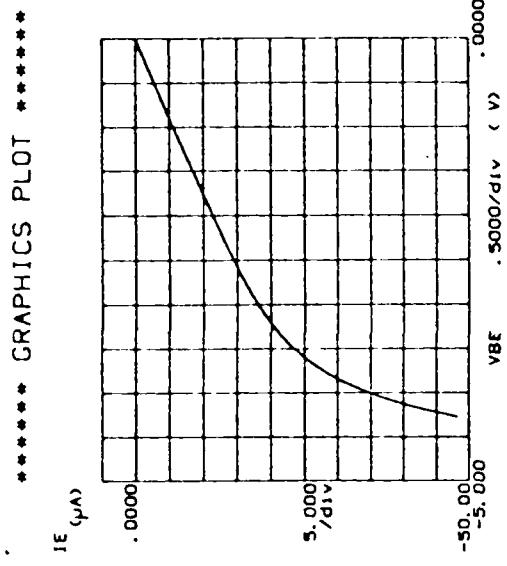
Figs. C.3.c



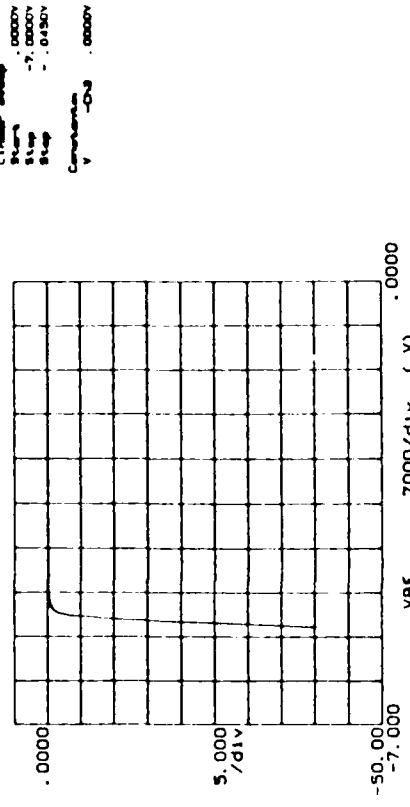
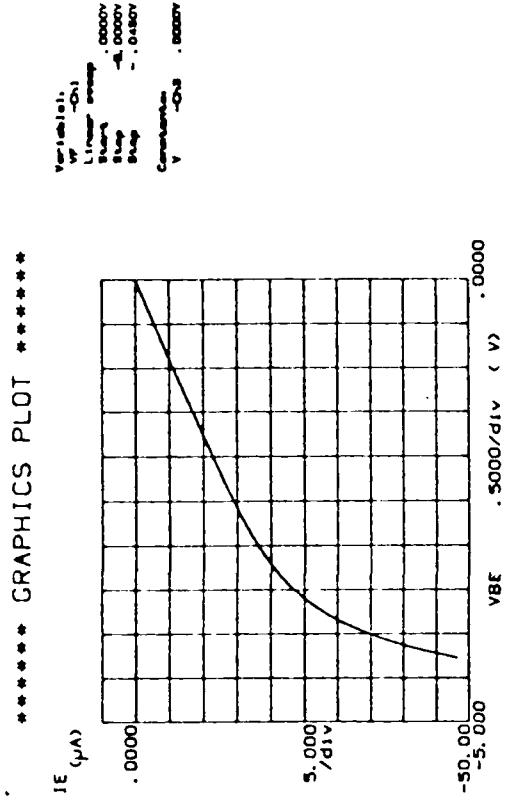
Plot 1 - 1C/10



Plot 2 - 1C/10



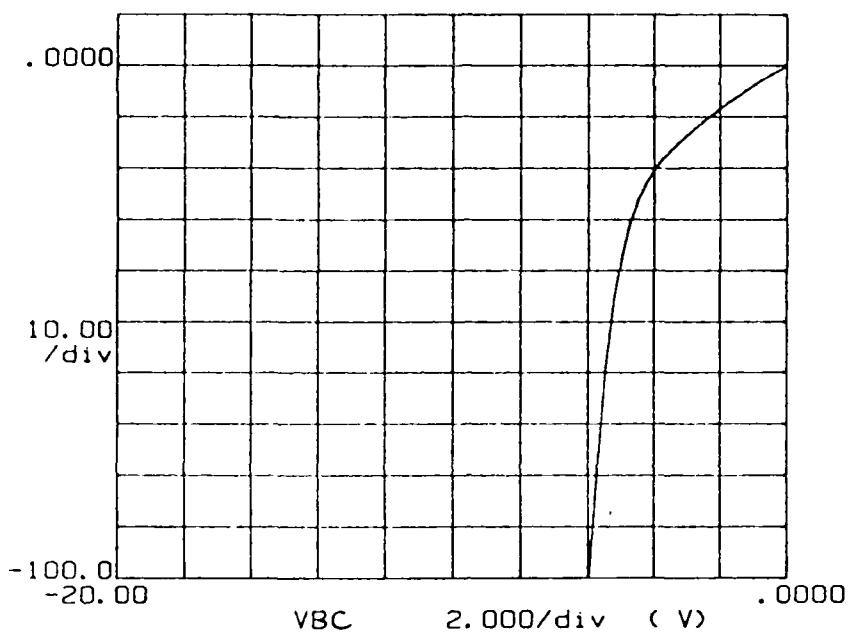
Plot 3 - 1C/10



Plot 4 - 1C/10

***** GRAPHICS PLOT *****

IC
(μ A)



Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop -20.000V
Step -.2500V

Constants:
V -Ch3 .0000V